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## Influence of source/drain residual implant lattice damage traps on silicon carbide metal semiconductor field effect transistor drain I-V characteristics

John Adjaye

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INFLUENCE OF SOURCE/DRAIN RESIDUAL IMPLANT LATTICE DAMAGE  
TRAPS ON SILICON CARBIDE METAL SEMICONDUCTOR FIELD EFFECT  
TRANSISTOR DRAIN I-V CHARACTERISTICS

By

John Adjaye

A Dissertation  
Submitted to the Faculty of  
Mississippi State University  
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TRAPS ON SILICON CARBIDE METAL SEMICONDUCTOR FIELD EFFECT  
TRANSISTOR DRAIN I-V CHARACTERISTICS

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Candidate for Degree of Doctor of Philosophy

4H-SiC n-channel power MESFETs with nitrogen-doped epitaxially grown channel and nitrogen  $n^+$ -implanted source/drain ohmic contact regions, with and without p-buffer layer fabricated on semi-insulating substrates exhibited hysteresis in the drain I-V characteristics of both types of devices at 300 K and 480 K due to traps. However, thermal spectroscopic measurements could detect the traps only in the devices without p-buffer.

In this study the two-dimensional device simulator, Medici<sup>TM</sup>, and optical admittance spectroscopy (OAS) measurements are used to help resolve the discrepancy in the initial experimental characterization results and interpret the results. Device simulations also showed hysteresis in the drain I-V curves of both types of devices at 300 K and 480 K. Simulations suggest that, in addition to the SI substrate traps, which are

known to be major cause of hysteresis in MESFET drain I-V characteristics, acceptor traps due to source/drain residual implant lattice damage could also contribute to the hysteresis observed in the drain I-V characteristics of the experimental MESFETs. Although surface traps are known to cause hysteresis in the I-V curves of MESFETs, their presence was not observed in the experimental devices.

The results of the OAS measurements showed several peaks in the spectra of the devices without p-buffer, while in the spectra of the devices with p-buffer the peaks were generally non-existent or reduced. This demonstrates that the peaks observed in the OAS spectra are largely due to substrate traps and that the p-buffer layer is effective in isolating the channel from the substrate. A peak centered around 1.51 eV below the conduction band, which has also been observed in the literature after He<sup>+</sup>-implantation, is consistently observed in the spectra of both types of devices although it appears reduced in the spectra of the devices with buffer. In this dissertation it is shown that it is likely the traps responsible for this peak could contribute to the hysteresis observed at 300 K and could be solely responsible for the hysteresis observed at high temperatures such as 480 K, since simulations suggest that hysteresis due to semi-insulating substrate traps disappear at high temperatures such as 480 K.

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# CHAPTER I

## INTRODUCTION

### 1.1 Background

Silicon carbide (SiC) metal semiconductor field effect transistors (MESFETs) continue to emerge as a viable alternative to other MESFETs such as GaAs MESFETs in such applications as high power, high frequency, high temperature, and high radiation environment. This is due to a number of superior properties of SiC, namely wide bandgap, high breakdown electric field, high saturation electron velocity, high thermal conductivity, and high radiation resistance [1, 2, 3]. For better performance characteristics, MESFETs have been fabricated on semi-insulating (SI) substrates with a p-type buffer layer between the active channel layer and the SI substrate [1, 2, 3, 4].

In order to fabricate planar devices in semiconductors, selective-area doping such as the doping of the source and drain ohmic contact regions of FETs, is required. For SiC, ion implantation is generally considered the major means of achieving selective-area doping due to the low diffusion coefficient of the major desirable dopants, i.e. N, P, B, and Al [5, 6, 7]. However, ion implantation leaves residual implant lattice damage, which has to be taken into account in device design and operation. Even after high temperature implantation and anneal, lattice damage still persists which leads to traps with energy levels distributed throughout the SiC band gap [5, 6, 7, 8, 9, 10, 11, 24, 26]. In particular,

ion implantation in 4H- and 6H-SiC causes point defects which lead to acceptor-like intrinsic deep level defect trap centers with energy levels distributed in the upper half of the band gap [8, 9]. It is quite plausible that these residual implant damage traps could lead to hysteresis (looping) in the drain I-V characteristic of MESFETs and other FETs in general.

Experimental characterization of 4H-SiC nitrogen-doped epitaxial n-channel power MESFETs with  $n^+$  nitrogen implanted source and drain ohmic contact regions, with and without p-buffer layer fabricated on semi-insulating substrates (a schematic of both types of devices is shown in Figures 4.1 and 4.2) showed hysteresis in the drain I-V characteristics of both the devices with buffer and those without buffer at 300 K and 480 K due to traps [12] to about the same degree. However, output thermal admittance spectroscopy (TAS), gate-source thermal conductance spectroscopy (TCS) and gate-source thermal deep level transient spectroscopy (DLTS) could detect the traps only in the devices without the p-buffer layer. The traps detected in the devices without p-buffer layer have activation energies in the range of  $(E_C - 0.95 \text{ eV})$  and  $(E_C - 1.08 \text{ eV})$  [12], which are consistent with vanadium acceptors in the semi-insulating substrate [8, 12, 53, 55, 56, 57, 58, 60, and 66].

In this study device simulation using the two-dimensional device simulator, Medici, and optical admittance spectroscopy (OAS) are used to help determine the origin of the hysteresis in both types of devices, eventhough traps were detected by thermal spectroscopic measurements only in the devices without p-buffer layer. Device simulations also exhibited hysteresis in the drain I-V characteristics of both the device

with buffer and the device without buffer at 300 K and 480 K. Simulations suggest that, in addition to the SI substrate traps, which are known to be a major cause of hysteresis in MESFET drain I-V characteristics [14 – 22], acceptor traps due to source and drain residual implant lattice damage can also be major contributors to the hysteresis observed in the drain I-V characteristics of the experimental MESFETs. Further simulations revealed that the hysteresis at 480 K could solely be due to the presence of acceptor-type deep level traps generated by the ion implantation used to form the source and drain ohmic contact regions with energy levels distributed in the 4H-SiC band gap.

Optical admittance spectroscopy (OAS) measurements showed several peaks in the spectra of the device without the p-buffer layer, which were either non-existent or reduced in the corresponding OAS spectra of the device with the p-buffer layer. This fact indicates that the observed peaks are mainly due to traps that are substrate related and that the p-buffer layer is effective in isolating the channel from the substrate. A peak centered at an optical wavelength of about 817 nm, which is equivalent to activation energy of ( $E_C - 1.51$  eV) is observed in the spectra of both the device without p-buffer layer and device with buffer layer. However, the peak in the spectra of the device with buffer is reduced relative to the corresponding peak in the spectra of the device without buffer. As will be shown later in this chapter, this peak corresponds to a trap with activation energy between ( $E_C - 1.49$  eV) and ( $E_C - 1.60$  eV) observed by T. Dalibor et al. (8) after  $\text{He}^+$ -implantation of n-type 4H-SiC CVD epitaxial layers. According to Dalibor et al., the defect traps responsible for the observed peak, which is labeled  $\text{RD}_4$  in Figure 1.6, are not related to He and are therefore intrinsic defects generated by the  $\text{He}^+$ -

implantation. It is quite plausible that the peak observed in the OAS spectra of both types of the experimental MESFETs could be due to traps generated by the  $N^+$ -implantation of the source and drain ohmic contact regions. Since a similar peak has been observed by Dalibor et al. (8) after  $He^+$ -implantation, it can be argued that the peak could be due to native point defects generated by any high-energy particle bombardment of the 4H-SiC material.

The fact that the 817 nm peak appears reduced in the spectra of the device with buffer relative to that in the spectra of the device without buffer can be explained by the observation that the p-buffer layer effectively screens any substrate traps. Furthermore, Koshka et al. [13] have shown that implant damage can extend beyond the projected range of implanted species. It is therefore plausible that the traps due to the source and drain implant damage extend into the substrate of both types of devices and that the p-buffer layer effectively screens the substrate portion of the traps in the device with p-buffer layer, revealing only the channel portion as an OAS peak, which is reduced in magnitude, compared to the corresponding peak in the spectra of the device without buffer.

Since hysteresis occurs in the drain I-V curves of both types of devices to about the same degree, the hysteresis could not be due mainly to substrate traps. Otherwise, the hysteresis would be more pronounced in the drain I-V curves of the devices without buffer than in the drain I-V curves of the devices with buffer. It can therefore be argued that the hysteresis observed in the drain I-V curves of both types of experimental devices is due largely to traps with similar parameters and concentrations either in the channel,

the surface or both. Device simulations demonstrate that the channel traps could be due to source/drain residual implant lattice damage, particularly in the lateral straggle areas in the un-gated channel regions. Although surface traps are believed to cause hysteresis in I-V curves of FETs, simulations with surface traps did not yield any hysteresis in the drain I-V curves of the MESFETs. Previous investigations into hysteresis in the drain I-V curves of MESFETs have mainly concentrated on semi-insulating substrate traps [14-22]. As a result hysteresis in the drain I-V characteristics of MESFETs have been largely attributed to semi-insulating substrate traps [14-22]. The thesis of this work is to show that traps due to source/drain residual implant lattice damage can at least contribute to the hysteresis in the drain I-V curves of MESFETs, and dominate at higher temperatures.

For the remainder of this chapter, section 1.2 discusses the presence of deep level traps in ion-implanted substrates and epilayers, section 1.3 contain a literature review of crystal damage and traps generated by ion-implantation and high-energy particle irradiation of bulk and epitaxial SiC, and section 1.4 briefly discusses the use of optical admittance spectroscopy (OAS) to detect deep level implant damage traps. Chapter II looks at the experimental set up and Chapter III discusses the initial experimental characterization of the devices, which motivated this work. The device simulations and their results are discussed in Chapter IV. In Chapter V the OAS measurements and OAS measurement results are presented, and Chapter VI presents discussions and conclusions.

## **1.2 Presence of Deep Level Traps in Ion-implanted Substrates and Epilayers**

As already mentioned above, previous experimental and quantitative investigations into hysteresis in drain I-V characteristics of MESFETs have mainly

concentrated on semi-insulating substrate traps [14-22]. As a result, hysteresis in drain I-V characteristics of MESFETs have been largely attributed to SI substrate traps [14-22]. It is, however, well established that ion implantation and any high-energy particle irradiation of bulk and epitaxial semiconductors generate lattice damage, resulting in the creation of traps with energy levels distributed in the semiconductor band-gap [5-11]. It is plausible that these implant damage induced traps could generate hysteresis in the drain I-V characteristics of FETs, as demonstrated by simulation. Although ion implantation is well known to cause lattice damage which leads to traps with energy levels distributed in the semiconductor band-gap, the possibility that these traps could contribute to hysteresis in drain I-V curves of FETs is typically overlooked in the literature. Since the  $n^+$  source and drain ohmic contact regions of the MESFETs that are the subject of this work were implanted, there will be residual implant lattice damage, which will lead to traps with energy levels distributed in the 4H-SiC band-gap as already pointed out above. These traps could be responsible for the hysteresis or at least contribute to the hysteresis in the drain I-V characteristics of the implanted MESFETs at both 300 K and 480 K. In addition to generating hysteresis in the I-V curves of FETs, the implant-induced deep level defect centers can act as trapping centers or recombination centers for electrons and/or holes, and thus limit the lifetime of the charge carriers with detrimental effect on their transport properties, which in the final analysis degrade device performance. Device performance characteristics that are degraded by the presence of traps are (1) device speed, (2) frequency response, (3) current levels, and hence power levels.

### 1.3 Literature Review of Crystal Damage and Traps Generated by Ion Implantation and High-Energy Particle Irradiation of Bulk and Epitaxial SiC

#### 1.3.1 M. V. Rao et al.: Ion-implantation in bulk semi-insulating 4H-SiC [5]

Rao et al. performed multiple energy ion implantation of nitrogen (N) at 500 °C and aluminum (Al) at 800 °C into bulk semi-insulating 4H-SiC at various doses to obtain uniform implant concentrations in the range of  $1 \times 10^{18} - 1 \times 10^{20} \text{ cm}^{-3}$  to a depth of about 1  $\mu\text{m}$ . The implanted samples were annealed at 1400, 1500, and 1600 °C for 15 minutes. The authors used Rutherford backscattering spectroscopy (RBS) with channeling measurements to evaluate the crystal quality of the as-implanted and annealed samples. Figure 1.1 shows the RBS spectra on virgin and N as-implanted bulk SI 4H-SiC for various N concentrations. The spectra are compared with the random spectrum.

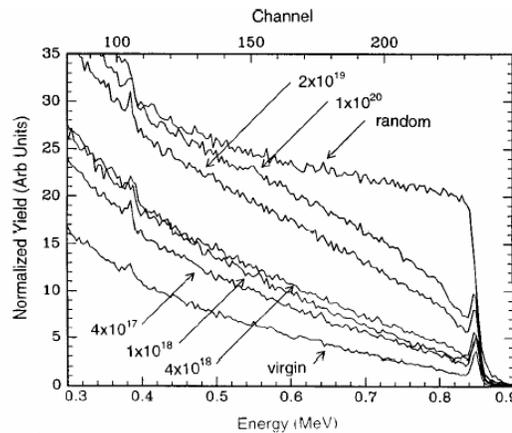


Figure 1.1: RBS spectra on virgin and nitrogen as-implanted, bulk semi-insulating 4H-SiC for various nitrogen concentrations [5]. The implantation is performed at 500 °C.

As can be seen, the RBS spectra of the implanted samples are between those of the virgin, un-implanted and random, amorphous samples, indicating that lattice damage occurs after ion implantation. Further more, Figure 1.1 shows that the lattice damage, measured as RBS yield, increases with increasing implant dose (concentration), with the lattice damage approaching that of the random sample. Figure 1.2 exhibits the RBS spectra on  $2 \times 10^{19} \text{ cm}^{-3}$  nitrogen implanted bulk SI 4H-SiC before and after 1400 °C and 1500 °C annealing. It can be observed from the figure that, even after high temperature N- implantation and high temperature annealing, lattice damage still remains, although lattice damage decreases with increasing annealing temperature.

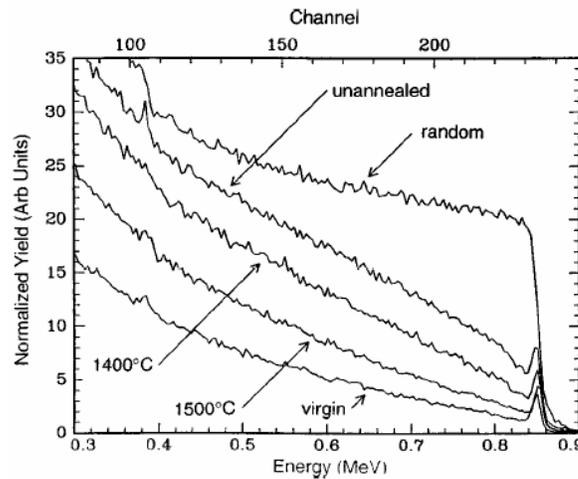


Figure 1.2: RBS spectra of N-implanted ( $500^\circ\text{C}$ ) bulk SI 4H-SiC sample before and after  $1400^\circ\text{C}$  and  $1500^\circ\text{C}$  annealing [5].

Figure 1.3 shows the RBS spectra of  $800^\circ\text{C}$  Al-implanted bulk SI 4H-SiC after  $1500^\circ\text{C}$  and  $1600^\circ\text{C}$  annealing. The implants were performed for a uniform  $1 \times 10^{19} \text{ cm}^{-3}$ , Al concentration to a depth of  $0.9 \mu\text{m}$ . As can be seen from the figure, the RBS spectra of the Al-implanted and annealed samples coincide with that of the virgin, un-implanted

sample, indicating a low degree of lattice damage. This leads the authors to make the observation that, Al implantation can be used to form high quality p-type SiC layers with reduced defect centers.

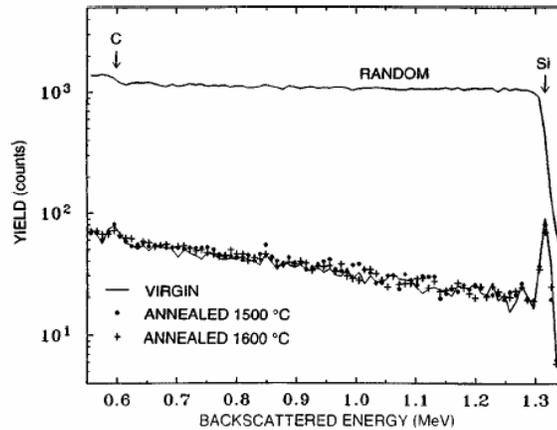


Figure 1.3: RBS spectra of 800 °C Al-implanted bulk 4H-SiC after 1500 °C and 1600 °C annealing [5].

Upon electrical characterization of the implanted materials, the authors observed a decreased room temperature sheet resistance ( $R_s$ ) and a corresponding increased sheet carrier concentration ( $n_s$ ) with increasing annealing temperature as shown in Figure 1.4, which shows the variation of room temperature sheet carrier concentration and sheet resistance for N-implant doses of  $2.28 \times 10^{15}$  and  $1.14 \times 10^{16} \text{ cm}^{-2}$ . They attribute this to the fact that more implant dopant atoms take substitutional sites (N atoms take substitutional C sites and Al atoms take substitutional Si sites) and compensating levels associated with implant damage decrease with increasing annealing temperature resulting in an improved  $n_s$  and corresponding decrease in  $R_s$ . The idea here is that, in order to achieve complete activation of the implanted dopant atoms, all the atoms have to occupy electrically active

substitutional lattice sites and residual lattice damage, which could otherwise compensate the activated dopant atoms, should be eliminated. It can be seen from Figure 1.4 that the sheet carrier concentration for the lower dose N-implant ( $2.28 \times 10^{15} \text{ cm}^{-2}$ ) is higher than that for the higher dose N-implant ( $1.14 \times 10^{16} \text{ cm}^{-2}$ ), resulting in a corresponding lower sheet resistance for the lower dose N-implant. The authors explain that for high implant doses the lattice damage is severe even for elevated temperature implantations and that this requires high post-implant annealing temperatures on the order of about  $1600 \text{ }^\circ\text{C}$  to achieve optimal electrical characteristics. They point out, however, that the surface morphology degrades for higher annealing temperatures due to the evaporation of Si containing species from the surface with increasing temperature. They observe that the damage is in the form of long furrows running in one direction across the wafer surface to a depth of  $\sim 25 \text{ nm}$  from the surface for samples annealed at  $1600 \text{ }^\circ\text{C}$  for 15 minutes.

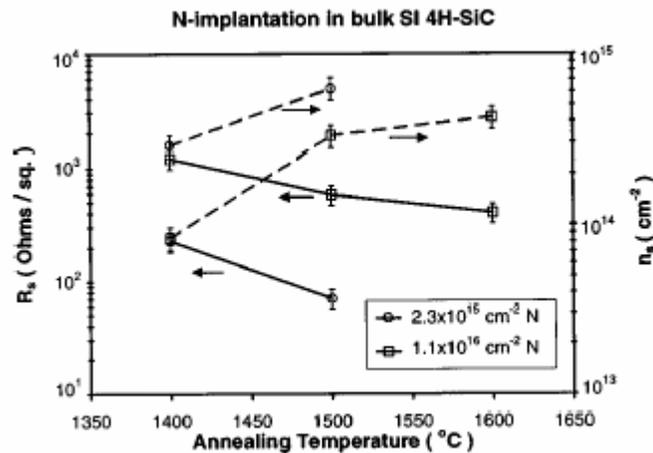


Figure 1.4: Variation of sheet resistance ( $R_s$ ) and sheet carrier concentration ( $n_s$ ) measured at room temperature with annealing temperature for two different doses of nitrogen implantations in bulk SI 4H-SiC [5].

In addition, they observed a general decrease in sheet resistance and corresponding increase in sheet carrier concentration with increasing implant dose due to increased concentration of implanted dopants, even though the N-implantation showed an increase in  $R_s$  and a corresponding decrease in  $n_s$  after an implant dose of  $\sim 2.28 \times 10^{15} \text{ cm}^{-2}$ , which the authors attribute to decrease in percentage activation (ratio of  $n_s$  to total dose,  $\Phi$ ) with increasing implant dose due to the presence of greater residual implant damage at higher doses. Figure 1.5 shows the variation of room temperature sheet carrier concentration and sheet resistance with N-implant dose for 1500 °C annealing for 15 minutes obtained by the authors.

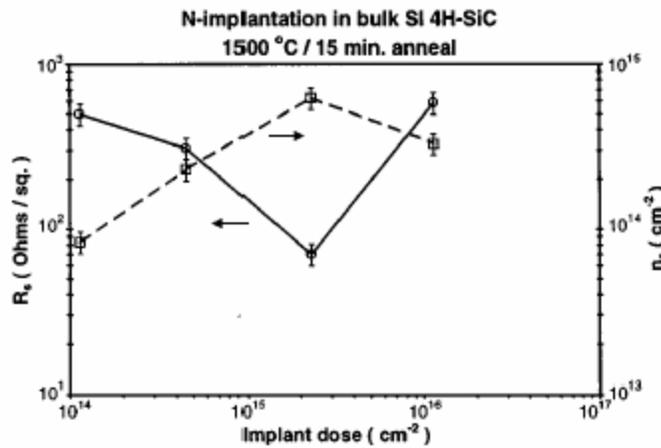


Figure 1.5: Variation of room temperature sheet carrier concentration ( $n_s$ ) and sheet resistance ( $R_s$ ) with N-implant dose for N-implanted bulk SI 4H-SiC after 1500 °C/15 min annealing measured by the authors [5].

From Figure 1.5 and as already mentioned above, the authors observe that the sheet carrier concentration for  $1.14 \times 10^{16} \text{ cm}^{-2}$  N implant dose is less than the value measured for the  $2.28 \times 10^{15} \text{ cm}^{-2}$  N implant. They again attribute this to the presence of more residual implant damage in the  $1.14 \times 10^{16} \text{ cm}^{-2}$ , N implanted material. In addition

the authors point out that the nitrogen concentration for the  $1.14 \times 10^{16} \text{ cm}^{-2}$  N dose is close to the solid solubility limit of N in SiC. Hence, Rao et al. further point out that N implant doping concentrations should be limited to values less than  $4 \times 10^{19} \text{ cm}^{-3}$  since no further benefit is achieved by using higher concentration. They observe that more residual lattice damage is created with possible penalty on electrical activation for higher implant doses. They further indicate that they measured 27% RT activation for  $2 \times 10^{19} \text{ cm}^{-3}$  N implantation.

### **1.3.2. T. Dalibor et al.: Deep Defect Centers in Silicon Carbide Monitored with Deep Level Transient Spectroscopy [8].**

Dalibor et al. [8] performed multiple, ion implantation on n-type 4H-SiC and 6H-SiC CVD epilayers using  $\text{He}^+$ ,  $\text{V}^+$ , and  $\text{Ti}^+$ . Figure 1.6 depicts the DLTS spectra of n-type 4H-SiC as-grown, CVD epilayer and after multiple  $\text{He}^+$ -implantation with total dose of  $9 \times 10^{10} \text{ cm}^{-2}$ , implant energy range of 30 – 650 keV, and anneals at 430 °C, 1000 °C, and 1400 °C. The implant profile depth was about 1.6  $\mu\text{m}$ .

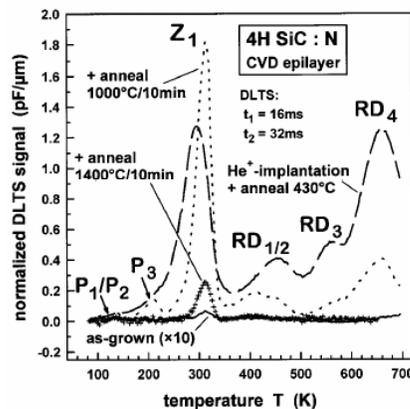


Figure 1.6: DLTS spectra of n-type 4H-SiC as-grown CVD epilayers and after  $\text{He}^+$ -implantation and anneals 430 °C, 1000 °C, and 1400 °C [8].

The trap parameters of the defect centers responsible for the DLTS peaks on the as-grown and He<sup>+</sup>-implanted and annealed n-type 4H-SiC CVD epilayers are shown in Table 1.1. The activation energies ( $\Delta E(i)$ ) and capture cross-sections ( $\sigma$ ) were obtained from Arrhenius analysis for  $\sigma$  independent of temperature and  $\sigma$  proportional to  $T^{-2}$ , respectively. From Figure 1.6 and Table 1.1, it can be noted that several defect trap centers are generated by the He<sup>+</sup>-implantation, with energy levels distributed in the upper half of the band gap, which are not related to He, the authors point out. Hence, these defect levels are intrinsic defects generated by the lattice damage due to the He<sup>+</sup>-implantation process. It is further observed that even after 1400 °C anneal, the Z<sub>1</sub> defect level still remains although its peak is reduced compared to the peaks after 430 °C and 1000 °C.

Table 1.1: Trap parameters of defect centers responsible for DLTS peaks on as-grown and He<sup>+</sup>-implanted and annealed n-type 4H-SiC CVD epilayers obtained from Arrhenius analysis for  $\sigma = \text{constant}$  and  $\sigma \propto T^{-2}$  obtained by Dalibor et al. [8].

peak temperature (K) ( $t_1/t_2$ = 16/32 ms)	center $i$	ionization energy $\Delta E(i)$ (eV)	capture cross section $\sigma(i)$ (cm <sup>2</sup> )	concentration $N(i)$ (cm <sup>-3</sup> )
135	P <sub>1</sub> /P <sub>2</sub>	0.19 to 0.21	$1 \times 10^{-17}$ to $1 \times 10^{-16}$	$1 \times 10^{14}$ (1000 °C anneal) $4 \times 10^{13}$ (1400 °C anneal)
210	P <sub>3</sub>	0.31 to 0.35	$2 \times 10^{-17}$ to $1 \times 10^{-16}$	$3 \times 10^{14}$ (1000 °C anneal)
310	Z <sub>1</sub>	0.63 to 0.68	$3 \times 10^{-15}$ to $2 \times 10^{-14}$	$2 \times 10^{13}$ (as-grown) $4 \times 10^{15}$ (430 °C anneal) $4 \times 10^{15}$ (1000 °C anneal) $3 \times 10^{14}$ (1400 °C anneal)
450	RD <sub>1/2</sub>	0.89 to 0.97	$7 \times 10^{-16}$ to $5 \times 10^{-15}$	$2 \times 10^{15}$ (430 °C anneal) $2 \times 10^{14}$ (1000 °C anneal) $4 \times 10^{13}$ (1400 °C anneal)
560	RD <sub>3</sub>	0.98 to 1.08	$5 \times 10^{-17}$ to $3 \times 10^{-16}$	$2 \times 10^{15}$ (430 °C anneal) $4 \times 10^{14}$ (1000 °C anneal)
660	RD <sub>4</sub>	1.49 to 1.60	$1 \times 10^{-14}$ to $9 \times 10^{-14}$	$4 \times 10^{15}$ (430 °C anneal) $4 \times 10^{14}$ (1000 °C anneal)

Figure 1.7 shows the DLTS spectra of as-grown (dashed curve), multiple  $\text{Ti}^+$ -implanted (solid curve), and multiple  $\text{V}^+$ -implanted (dotted curve) n-type 4H-SiC CVD epilayers. The total implant dose and energy range of both the  $\text{Ti}^+$  and  $\text{V}^+$  implants were  $2 \times 10^{12} \text{ cm}^{-2}$  and 450 – 1900 keV respectively. The depth profiles of both implants were 1.2  $\mu\text{m}$ . The implanted epilayers were annealed at 1700 °C for 30 minutes. Table 1.2 shows the trap parameters of the defect levels detected by Dalibor et al. in the  $\text{Ti}^+$ - and  $\text{V}^+$ -implanted and annealed n-type 4H-SiC CVD epilayers. The trap parameters were obtained from Arrhenius analysis of the DLTS data assuming temperature independent capture cross-section ( $\sigma$ ) and  $\sigma \propto T^{-2}$ .

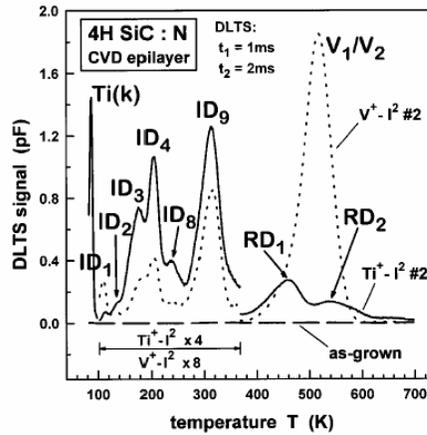


Figure 1.7: DLTS spectra of as-grown (dashed curve),  $\text{Ti}^+$ -implanted (solid curve),  $\text{V}^+$ -implanted (dotted curve) n-type 4H-SiC CVD epilayers [8].

Table 1.2: Trap parameters of defect centers detected in Ti<sup>+</sup>- and V<sup>+</sup>-implanted and annealed n-type 4H-SiC CVD epilayers obtained by Dalibor et al. [8].

peak temperature (K) ( $t_1/t_2 = 1/2$ ms)	center $i$	ionization energy $\Delta E(i)$ (eV)	capture cross section $\sigma(i)$ (cm <sup>2</sup> )
110	ID <sub>1</sub>	0.16 to 0.18	$6 \times 10^{-16}$ to $4 \times 10^{-15}$
135	ID <sub>2</sub>	0.19 to 0.21	$2 \times 10^{-16}$ to $1 \times 10^{-15}$
178	ID <sub>3</sub>	0.26 to 0.29	$1 \times 10^{-16}$ to $1 \times 10^{-15}$
205	ID <sub>4</sub>	0.32 to 0.35	$6 \times 10^{-16}$ to $9 \times 10^{-15}$
238	ID <sub>5</sub>	0.44 to 0.48	$2 \times 10^{-14}$ to $1 \times 10^{-13}$
317	ID <sub>9</sub>	0.52 to 0.57	$9 \times 10^{-16}$ to $7 \times 10^{-15}$
460	RD <sub>1</sub>	0.90 to 0.97	$8 \times 10^{-15}$ to $6 \times 10^{-14}$
540	RD <sub>2</sub>	0.92 to 1.01	$5 \times 10^{-16}$ to $3 \times 10^{-15}$

It can be observed again that, ion implantation of Ti and V into n-type 4H-SiC generate several trap levels in the upper half of the 4H-SiC band gap due to the implant lattice damage. In addition, the authors note that defect centers ID<sub>1</sub> to ID<sub>4</sub>, ID<sub>8</sub> and ID<sub>9</sub> appear in both the Ti<sup>+</sup>- and V<sup>+</sup>-implantation DLTS spectra in addition to the peaks Ti(k) and V<sub>1</sub>/V<sub>2</sub>, which are related to titanium and vanadium respectively, and are therefore intrinsic defects.

The authors performed double-correlation DLTS (DDLTS) on the n-type 4H-SiC CVD epilayer upon V<sup>+</sup>-implantation and annealing at 1700 °C for three different applied E-fields varying from  $3 \times 10^4$  to  $1 \times 10^5$  V/cm, to determine the final charge state of the defect trap levels. Figure 1.8 shows the DDLTS spectra of the above-mentioned sample.

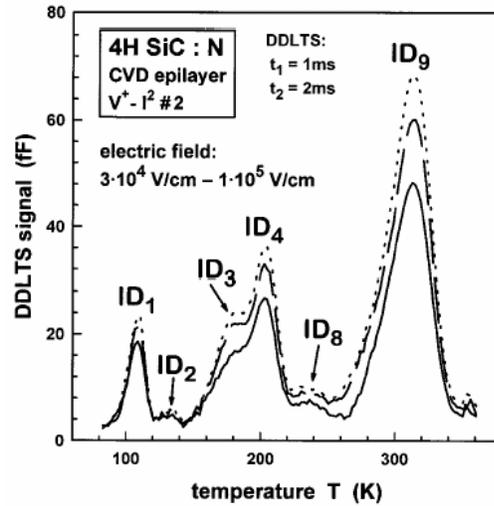


Figure 1.8: Double-correlation DLTS (DDLTS) spectra for n-type 4H-SiC CVD epilayers upon  $V^+$ -implantation and anneal at 1700 °C for three different applied E-fields varying from  $3 \times 10^4$  to  $1 \times 10^5$  V/cm [8].

It can be noted that the temperature positions of the DLTS peaks do not change with varying electric field, indicating that the ionization energies of the defect centers are independent of electric field. The authors therefore deduce that the final charge state of defect levels is neutral, and hence, ID<sub>1</sub> to ID<sub>4</sub>, ID<sub>8</sub> and ID<sub>9</sub> are acceptor-like according to the relation  $A^- = A^0 + e^-$ . A summary of ground state of the intrinsic deep defect trap centers in the n-type 4H-SiC epilayer obtained from DLTS investigations conducted by Dalibor et al. and other authors is shown in Figure 1.9. The trap energy levels used were obtained from Arrhenius analysis based on temperature independent capture cross-section, that is  $\sigma = \text{constant}$ .

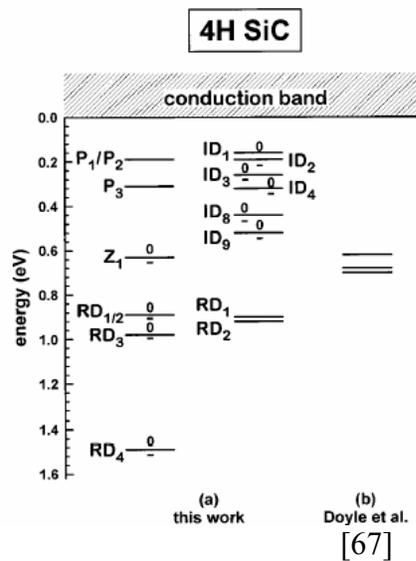


Figure 1.9: Summary of ground state of intrinsic defect levels in n-type 4H-SiC epilayers obtained from DLTS investigations conducted by Dalibor et al. and other authors [8].

Dalibor et al. also performed  $\text{He}^+$ ,  $\text{Ti}^+$ , and  $\text{V}^+$ -implantation in n-type 6H-SiC CVD epilayers, which were subsequently annealed at various temperatures (430 °C, 1000 °C, and 1700 °C). The authors then used DLTS measurements to investigate the traps generated by the ion implantation process. Tables 1.3 shows the trap parameters of the defect centers detected in the DLTS spectra of as-grown and  $\text{He}^+$ -implanted and annealed n-type 6H-SiC CVD epilayers assuming  $\sigma = \text{constant}$  and  $\sigma \propto T^{-2}$ . The trap parameters of defect centers observed in the DLTS spectra of the  $\text{Ti}^+$ - and  $\text{V}^+$ -implanted and annealed (1700 °C for 30 minutes) n-type 6H-SiC CVD epilayers are shown in Table 1.4 for  $\sigma = \text{constant}$  and  $\sigma \propto T^{-2}$  respectively.

Table 1.3: Trap parameters of the defect centers observed in the DLTS spectra of as-grown and He<sup>+</sup>-implanted and annealed n-type 6H-SiC CVD epilayers assuming  $\sigma = \text{constant}$  and  $\sigma \propto T^{-2}$  obtained by Dalibor et al. [8].

peak temperature (K) ( $t_1/t_2 = 16/32$ ms)	center $i$	ionization energy $\Delta E(i)$ (eV)	capture cross section $\sigma(i)$ (cm <sup>2</sup> )	concentration $N(i)$ (cm <sup>-3</sup> )
120		0.18 to 0.20	$4 \times 10^{-17}$ to $3 \times 10^{-16}$	$1 \times 10^{14}$ (1000 °C anneal)
195	E <sub>1</sub> /E <sub>2</sub>	0.39 to 0.43	$7 \times 10^{-15}$ to $5 \times 10^{-14}$	$2 \times 10^{13}$ (as-grown) $3 \times 10^{15}$ (430 °C anneal) $3 \times 10^{15}$ (1000 °C anneal) $4 \times 10^{14}$ (1700 °C anneal)
230	RD <sub>5</sub>	0.43 to 0.47	$1 \times 10^{-15}$ to $9 \times 10^{-15}$	$3 \times 10^{15}$ (as-implanted)
310/330	Z <sub>1</sub> /Z <sub>2</sub>	0.65 to 0.72	$2 \times 10^{-15}$ to $1 \times 10^{-14}$	$3 \times 10^{15}$ (as-implanted) $9 \times 10^{14}$ (430 °C anneal) $4 \times 10^{14}$ (1000 °C anneal) $1 \times 10^{14}$ (1700 °C anneal)
540	R	1.17 to 1.27	$5 \times 10^{-15}$ to $3 \times 10^{-14}$	$2 \times 10^{13}$ (as-grown) $4 \times 10^{15}$ (as-implanted) $4 \times 10^{15}$ (430 °C anneal) $1 \times 10^{14}$ (1000 °C anneal)

Table 1.4: Trap parameters of defect centers detected in Ti<sup>+</sup>- or V<sup>+</sup>-implanted n-type 6H-SiC CVD epilayers annealed at 1700°C for 30 minutes for  $\sigma = \text{constant}$  and  $\sigma \propto T^{-2}$  obtained by Dalibor et al. [8].

peak temperature (K) ( $t_1/t_2 = 1/2$ ms)	center $i$	ionization energy $\Delta E(i)$ (eV)	capture cross section $\sigma(i)$ (cm <sup>2</sup> )
155	ID <sub>5</sub>	0.27 to 0.30	$4 \times 10^{-15}$ to $3 \times 10^{-14}$
209	ID <sub>6</sub>	0.40 to 0.43	$2 \times 10^{-14}$ to $1 \times 10^{-13}$
254	ID <sub>7</sub>	0.50 to 0.54	$4 \times 10^{-14}$ to $3 \times 10^{-13}$
364	Z <sub>1</sub> /Z <sub>2</sub>	0.62 to 0.67	$3 \times 10^{-15}$ to $2 \times 10^{-14}$

In addition to the traps in Tables 1.3 and 1.4, the authors also observed the V<sub>1</sub>/V<sub>2</sub> and V<sub>3</sub> trap centers, which they attribute to the vanadium. They further relate the Z<sub>1</sub>/Z<sub>2</sub> center to titanium, while they attribute the ID<sub>5</sub>-ID<sub>7</sub> centers to implantation-induced intrinsic defect centers. Double correlation DLTS measurements by the authors reveal that the traps in Table 1.3 are acceptor-like according to the relation,  $A^- = A^0 + e^-$ . Figure

1.10 shows the summary of ground state intrinsic defect centers in the He<sup>+</sup>-, Ti<sup>+</sup>-, V<sup>+</sup>-implanted 6H-SiC CVD epilayers obtained from DLTS investigations conducted by Dalibor et al. and several other authors based on Arrhenius analysis for temperature independent capture cross-section, i.e.  $\sigma = \text{constant}$ .

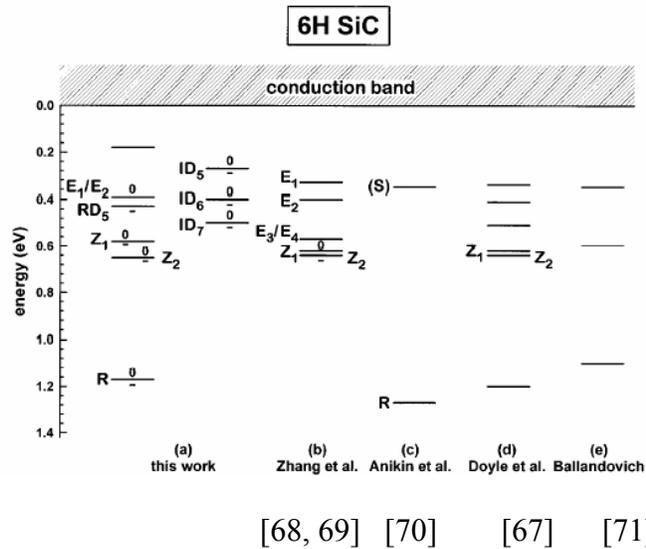


Figure 1.10: Summary of ground state of intrinsic defect centers in 6H-SiC obtained from DLTS measurements conducted by Dalibor et al. and other authors based on Arrhenius analysis for  $\sigma = \text{constant}$  [8].

According to Patrick et al. [23], He ions penetrate deep into an implanted substrate and do not contribute to photoluminescence (PL) spectrum of SiC samples bombarded with He ions. They based their observation on the fact that He ions do not play any part in luminescence by observing the same PL spectrum in samples bombarded with Ne, Ar, Ag, and I. Patrick et al. also observed the same PL spectrum on samples bombarded with 1-MeV electrons at a dose of  $6 \times 10^{17} \text{ cm}^{-2}$  in a Van de Graaff accelerator. This seems to be borne out by the experiments of Dalibor et al. since the He ions did not

generate any DLTS peaks but only the damage created by  $\text{He}^+$ -implantation resulted in DLTS peaks.

### **1.3.3. T. Troffer et al.: Doping of SiC by Implantation of Boron and Aluminum [9]**

Troffer et al. investigated  $\text{Al}^+$ - and  $\text{B}^+$ -implanted n-type and p-type 4H- and 6H-SiC epilayers with DLTS measurements and observed that no defect levels are found in the  $\text{Al}^+$ -implanted p-type 4H- and 6H-SiC epilayers. In the  $\text{B}^+$ -implanted p-type 4H- and 6H-SiC epilayers, the authors observed the well-known D-center with peak DLTS signal temperature position at approximately 300 K. A series of defect centers were, however, generated by the  $\text{Al}^+$ - and  $\text{B}^+$ -implantation in the n-type 4H- and 6H-SiC epilayers. Figure 1.11 shows the DLTS spectra of  $\text{Al}^+$ - and  $\text{B}^+$ -implanted n-type 4H-SiC samples (solid curves) annealed at 1700 °C for 30 minutes. The authors attribute the observed DLTS peaks to intrinsic defects. They indicate that similar DLTS spectra were observed for the  $\text{Al}^+$ - and  $\text{B}^+$ -implanted n-type 6H-SiC samples.

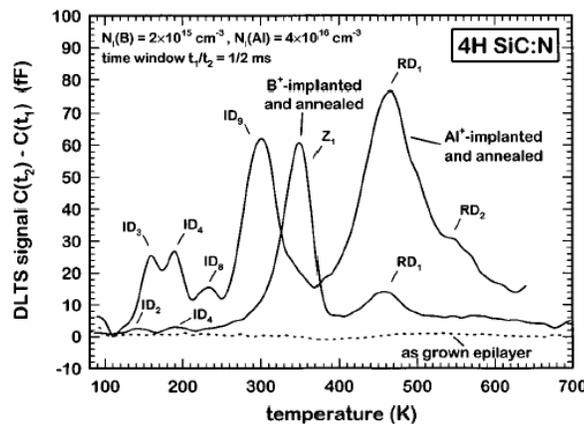


Figure 1.11: DLTS spectra of  $\text{Al}^+$ - and  $\text{B}^+$ -implanted n-type 4H-SiC epilayers (solid curves) annealed at 1700 °C for 30 minutes [9].

Table 1.5 shows the trap parameters of defect centers observed in the n-type 4H-SiC Al<sup>+</sup>-implanted epilayers. It should be noted that the same defect centers observed by Troffer et al. were also detected by Dalibor et al. after Ti<sup>+</sup>- and V<sup>+</sup>-implantation of n-type 4H- and 6H-SiC epilayers. This indicates that these defect centers are implant species independent and are therefore intrinsic defects.

Table 1.5: Trap parameters of defect centers detected in the n-type 4H-SiC Al<sup>+</sup>-implanted epilayers obtained by Troffer et al. [9].

defect center	concentration $N$ (cm <sup>-3</sup> )	ionization energy $\Delta E$ (meV) ( $\sigma \propto T^{0/-2}$ )	capture cross section $\sigma$ ( $\propto T^{0/-2}$ )
ID <sub>1</sub>	$7 \times 10^{13}$	96/112	$6 \times 10^{-18}/4 \times 10^{-17}$
ID <sub>3</sub>	$2 \times 10^{14}$	223/250	$1 \times 10^{-16}/9 \times 10^{-16}$
ID <sub>4</sub>	$2 \times 10^{14}$	270/302	$2 \times 10^{-16}/1 \times 10^{-15}$
ID <sub>8</sub>	$6 \times 10^{13}$	337/375	$1 \times 10^{-16}/8 \times 10^{-16}$
ID <sub>9</sub>	$6 \times 10^{14}$	415/465	$3 \times 10^{-17}/2 \times 10^{-16}$
RD <sub>1</sub>	$1 \times 10^{16}$	700/777	$7 \times 10^{-17}/5 \times 10^{-16}$

The trap parameters of defect centers detected in B<sup>+</sup>-implanted n-type 4H-SiC epilayers are shown in Table 1.6. It can be noted, once again that, the same defect centers shown in Table 1.6 were also detected by Dalibor et al., after Ti<sup>+</sup>- and V<sup>+</sup>-implantation of n-type 4H- and 6H-SiC epilayers. Troffer et al. therefore conclude that these are intrinsic defect centers with varying composition and/or structure. It can further be noted that Dalibor et al. have shown these traps to be acceptor-like based on the results of their double correlation DLTS investigations.

Table 1.6: Trap parameters of defect centers observed in n-type 4H-SiC B<sup>+</sup>-implanted epilayers obtained by Troffer et al. [9].

defect center	concentration $N$ (cm <sup>-3</sup> )	ionization energy $\Delta E$ (meV) ( $\sigma \propto T^{0/-2}$ )	capture cross section $\sigma$ ( $\propto T^{0/-2}$ )
ID <sub>2</sub>	$2 \times 10^{13}$	192/216	$1 \times 10^{-16}/1 \times 10^{-15}$
ID <sub>4</sub>	$2 \times 10^{14}$	264/298	$2 \times 10^{-17}/2 \times 10^{-16}$
Z <sub>1</sub>	$1 \times 10^{15}$	603/660	$1 \times 10^{-16}/1 \times 10^{-15}$
RD <sub>1</sub>	$2 \times 10^{14}$	752/826	$1 \times 10^{-16}/8 \times 10^{-16}$

#### **1.3.4. Kimoto et al.: Nitrogen Ion Implantation into $\alpha$ -SiC Epitaxial Layers [7]**

Kimoto et al. [32] performed N<sup>+</sup> implantation into  $\alpha$ -SiC (4H-SiC and 6H-SiC) at room temperature (RT), 500 °C, and 800 °C with total dose of  $4 \times 10^{15}$  cm<sup>-2</sup>. Using RBS measurements with channeling to analyze the implantation-induced damage, they observed that in the case of the RT implant, the aligned yield of the damaged region with channel numbers 230 to 280 reached the random yield, demonstrating high implant-induced damage. However, the RBS yield decreased with increasing implantation temperature, indicating that implantation-induced lattice damage is reduced by hot (high temperature) implantation. The yields for most part of the RT implant, 500 °C and 800 °C implants are less than that of random sample but greater than that of the virgin sample, even though the yields for the 500 °C and 800 °C implants are much closer to virgin sample yield. This indicates that implantation-induced lattice damage still persist even when hot implantation is used. The authors further observed that for RT implants, when the dose exceeded  $4 \times 10^{15}$  cm<sup>-2</sup>, the normalized yield  $\chi$ , which is the ratio of the aligned yield in the damaged region to that of the random yield, before annealing reached 100%,

which indicates that a completely amorphous region is formed. Even after 1500 °C annealing, substantial damage still remained in the RT implanted sample. However, upon hot implantation, the authors observed that the  $\chi$  of the as-implanted samples could be kept below 20% and that annealing at 1500 °C reduced  $\chi$  values to between 2 and 3%, which is close to the virgin sample  $\chi$  value of ~2%. Hence hot implantation coupled with high temperature anneal can help reduce implant-induced lattice damage substantially. Kimoto et al. further suggest that implant-induced lattice damage results in point defects and point defect clusters but the extremely small diffusion coefficient of point defects in SiC suppresses the formation of extended defects, such as dislocation loops and stacking faults. They also point out that, any high-energy particle irradiation of 6H-SiC generates the well-known  $Z_1/Z_2$  centers with energy levels of  $E_C - 620/640$  eV. Kimoto et al. observed a decrease in sheet resistance and a corresponding increase in electrical activation with annealing temperature as observed by Rao et al.

#### **1.3.5. A. Hallen et al.: Ion Implantation Induced Defects in Epitaxial 4H-SiC [24]**

Hallen et al. implanted n-type 4H-SiC epitaxial layers with low doses of 1.7 MeV He and 5.0 MeV B. The epilayer doping concentration was  $1 \times 10^{15} \text{ cm}^{-3}$  and the implant doses were between  $5 \times 10^8$  and  $1 \times 10^{10} \text{ cm}^{-2}$  for He and between  $2 \times 10^8$  and  $3 \times 10^9 \text{ cm}^{-2}$  for B, with the dose rate fixed around,  $5 \times 10^8 \text{ s}^{-1} \text{ cm}^{-2}$  for both He and B. The implant energies were selected to give the same implantation depth for the two ions, which was about 4  $\mu\text{m}$ , as predicted by their TRIM simulations. The implantations were carried out at room temperature with the exception of one of the samples, which was implanted with

$8 \times 10^8 \text{ B cm}^{-2}$  at  $700 \text{ }^\circ\text{C}$ . Selected groups of the samples were annealed at 700, 800, and  $1000 \text{ }^\circ\text{C}$  for 30 minutes. Schottky contacts were formed on the samples by evaporation of Au dots with a diameter of 0.8 mm using a metal mask under a base pressure of  $5 \times 10^{-5}$  Torr, after the samples were cleaned with trichloroethylene, acetone, and ethanol and dipped into 10% HF solution. The authors then used capacitance-voltage (C-V) and deep level transient spectroscopy (DLTS) to characterize the samples, with the DLTS measurements being performed within the temperature range of 77 K and 350 K.

Figure 1.12 compares the doping concentrations extracted from C-V measurements for  $2 \times 10^9 \text{ cm}^{-2}$  He implantations in Si and SiC. A distorted doping profile typical of a highly compensated material is observed for the SiC sample. The authors assert that if acceptor traps and a highly inhomogeneous trap distribution are present as in the case of an ion implanted sample, this will lead to an anomalous increase in doping concentration, as proven by Kimerling [25]. Hence the increase in  $N_{\text{eff}}$  at  $4.1 \text{ } \mu\text{m}$  is a measurement artifact, which indicates the presence of acceptor traps [24]. It can be seen from Figure 1.12 that for depths less than  $4 \text{ } \mu\text{m}$  the background doping  $N_{\text{D}}$  is reduced by implantation induced lattice damage traps, which results in an effective doping concentration,  $N_{\text{eff}}$ , less than the doping concentration,  $N_{\text{D}}$ , with a minimum occurring around where the maximum elastic energy deposition occurs, i.e. where the most lattice damage occurs, as suggested by the authors. They further observe that there is only a small trace of compensation at the mean projected range of  $5.8 \text{ } \mu\text{m}$  for the silicon sample and that the small dip at  $3.3 \text{ } \mu\text{m}$  in the silicon curve is not associated with the compensation.

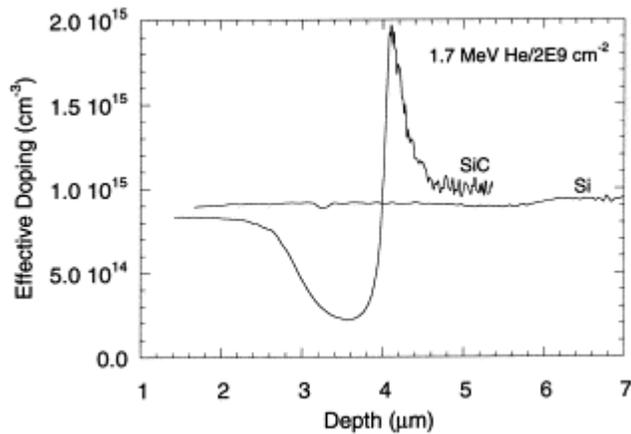


Figure 1.12: Comparison of  $2 \times 10^9 \text{ cm}^{-2}$  He implantation in Si and SiC. The distortion in the SiC doping profile is typical of highly compensated material. The background doping is reduced by implant damage traps and an effective doping is measured. The increased doping at  $4.1 \mu\text{m}$  indicates the presence of acceptor traps [24].

The authors observe from the results of their experiments that ions stopped in SiC produce five times or more room temperature stable point defects than the same ions do in Si. They go on to explain that one reason for the high number defects formed in SiC is that SiC is a compound semiconductor while Si is an elemental material. As a result in SiC, interstitial atoms generated by the implantation process can be either carbon or silicon while in silicon the interstitials are only silicon atoms. Another reason for the presence of high-density point defects in SiC relative to Si is that the diffusivity of the defects is lower in SiC than in Si, which reduces the immediate recombination of the defects in SiC. The authors further state that due to high density of defects in SiC relative to Si for the same implantation schedule, it will be more difficult to obtain implanted SiC pn-junction of the same high quality as found in Si technology.

Figure 1.13 shows C-V profiles for an un-implanted sample, a room temperature implanted sample using,  $2 \times 10^9$  He  $\text{cm}^{-2}$  and a 700 °C implanted sample using  $8 \times 10^8$  B  $\text{cm}^{-2}$ . The authors point out that the room temperature  $2 \times 10^9$  He  $\text{cm}^{-2}$  and the 700 °C  $8 \times 10^8$  B  $\text{cm}^{-2}$  were compared because they give the same maximum number of vacancies according to their TRIM simulations. This was done, they say, because the  $8 \times 10^8$  B  $\text{cm}^{-2}$  room temperature implantation malfunctioned. They observe from Figure 1.13 that the compensation, or point defect formation, in the high temperature implanted sample is substantially lower than in the room temperature implanted sample.

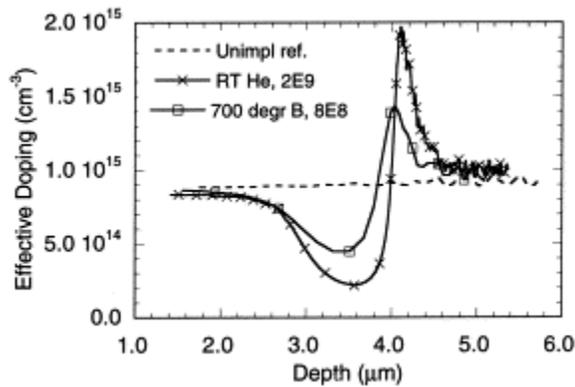


Figure 1.13: C-V profiles of an un-implanted sample, a room temperature implanted sample using  $2 \times 10^9$  He  $\text{cm}^{-2}$ , and a 700 °C implanted sample using  $8 \times 10^8$  B  $\text{cm}^{-2}$ . The authors point out that the two implantations give the same maximum number of vacancies according to their TRIM simulations, however, the hot implant shows much less compensation [24].

Figure 1.14 depicts three C-V profiles, one of an as-implanted sample, using  $2 \times 10^9$  He  $\text{cm}^{-2}$ , another after 700 °C anneal, and one other after 1000 °C anneal. The authors observe that the major part of the implant damage recovery seems to take place

during the 700 °C anneal and that increasing the temperature to 1000 °C does not substantially alter the C-V profile.

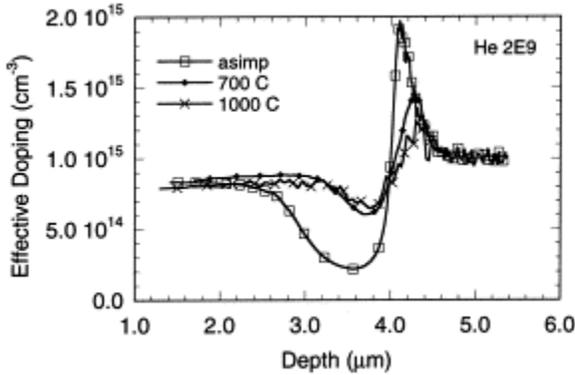


Figure 1.14: C-V profiles of a sample implanted at room temperature with  $2 \times 10^9$  He  $\text{cm}^{-2}$  and after 700 °C and 1000 °C anneals for 30 minutes [24].

From the above observations it can be seen that even after high temperature implantation and anneal implant lattice damage still remains as manifested by the compensation in the C-V doping profiles. The DLTS temperature spectra of an unimplanted reference sample and a room temperature  $2 \times 10^8$  B  $\text{cm}^{-2}$  implanted sample obtained by the authors is shown in Figure 1.15. They determined the energy positions of the two peaks to be  $E_C - 0.18$  eV and  $E_C - 0.67$  eV ( $\pm 0.03$  eV). They point out that the two peaks are intrinsic in nature since they grow after implantation. They make the observation that on the high temperature side of the  $E_C - 0.67$  eV peak, a shoulder appears that may originate from another defect. The authors further observe that annealing up to 1000 °C does not significantly change the concentration of the  $E_C - 0.67$  eV peak, suggesting that it may be the  $Z_1$  defect center, which is known to be stable even at 2000 °C as also observed by Dalibor et al. [8]. They point out that deeper lying

acceptor traps that anneal out at temperatures below 700 °C and were not seen in their measurement since they were restricted to 350 °C are responsible for the major part of the doping compensation.

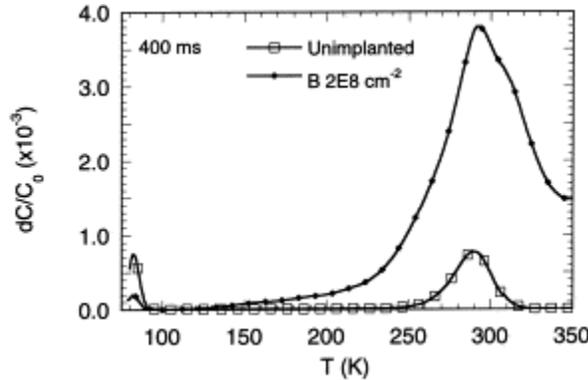


Figure 1.15: DLTS temperature spectra of an un-implanted sample and a room temperature  $2 \times 10^8 \text{ B cm}^{-2}$  implanted sample with a rate window of 400 ms long [24].

### **1.3.6. B. G. Svensson et al.: Doping of Silicon Carbide by Ion Implantation [26]**

Svensson et al. implanted n-type low-doped high purity 4H- and 6H-SiC epitaxial layers with  $^4\text{He}$ ,  $^{11}\text{B}$ , or  $^{27}\text{Al}$  ions similar to that performed by Hallen et al. The doping concentration of the epilayers was between  $1 \times 10^{15}$  and  $5 \times 10^{15} \text{ cm}^{-3}$ . They used wide dose range from  $1 \times 10^9$  to  $1 \times 10^{15} \text{ cm}^{-2}$  and energy range from 100 keV to 5 MeV and the implantation temperatures were between 25 °C (room temperature (RT)) and 800 °C.

Figure 1.16 shows a comparison of the charge carrier concentrations, obtained with 1 MHz C-V measurements, in 4H-SiC and Si samples implanted at room temperature with 1.7 MeV He ions to a dose of  $2 \times 10^9 \text{ cm}^{-2}$ . Both samples had a free and uniform electron concentration of  $0.9 \times 10^{15}$  to  $1 \times 10^{15} \text{ cm}^{-3}$  before implantation. The plot in Figure 1.16 is similar to the one obtained by Hallen et al. [24] shown in Figure 1.12.

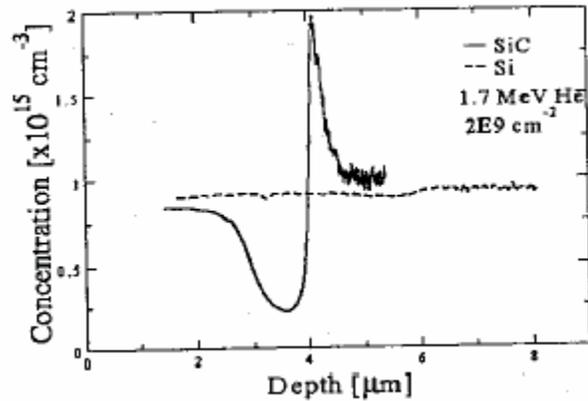


Figure 1.16: Comparison of carrier concentration profiles in n-type SiC and Si samples after He ion implantation at RT [26].

For this low dose implantation, the authors observe that a strong compensation of about 80% occurs in the SiC sample at the implantation damage peak depth of approximately 3.6  $\mu\text{m}$ . In the Si sample, only a small compensating effect is observed at the peak implant damage position of about 5.6  $\mu\text{m}$ . The authors refer to the apparent increase in doping with a maximum at a depth of about 4.1  $\mu\text{m}$  as a measurement artifact indicative of deep acceptor traps. They point out that this is due to contributions from both the leading and trailing edges of the Debye tail to the measured capacitance as already determined by Kimerling [26] and also pointed out by Hallen et al. The authors further indicate that the plot in Figure 1.16 shows a maximum compensation of about  $8 \times 10^{14} \text{ cm}^{-3}$  in the SiC sample and about  $1 \times 10^{14} \text{ cm}^{-3}$  in the Si sample, indicating that the generation rate of compensating defects is roughly a factor of 5 to 10 times higher in SiC than in Si. They go on to say that for silicon, it is known from their previous investigations that only a small percentage of the implantation-induced vacancies and self-interstitials survive immediate recombination at RT and form stable defects at low

doses, which is obviously not the case for SiC and they put forward different explanations. They point out that first, SiC is a compound semiconductor and anti-site defects, that is, silicon on carbon site and carbon on silicon site, are likely to form during recombination between vacancies and self-interstitials. Secondly, they further point out, the mobility of vacancies and self-interstitials is low in SiC and this reduces the probability for recombination relative to that in Si.

Svensson et al. note that for low dose implantation such as  $1 \times 10^{10} \text{ cm}^{-2}$  and below, the compensation does not show any dependence on implantation temperature between RT and 600 °C. They point out that this suggests that the mobility of vacancies, which promotes defect recombination, has little influence on the compensation effect. At higher doses (doses between  $1 \times 10^{14}$  and  $1 \times 10^{15} \text{ cm}^{-2}$ ), however, the authors observe that the rate of defect recombination increases substantially during hot implants at temperatures 200 °C and greater. In these high-dose, high-temperature implanted samples the authors identified one type of structural defect that dominates after post-implant anneals at 1700 - 2000 °C. They identified the defect as a dislocation loop composed of clustered interstitial atoms inserted on the basal plane of the hexagonal crystal structure.

### **1.3.7. S. Mitra et al.: Deep levels in ion implanted field effect transistors on SiC [10]**

S. Mitra et al. fabricated n-channel MESFETs ( $W/L = 280/2 \text{ }\mu\text{m}$ ) on Si-face,  $8^\circ$  off-axis, semi-insulating (SI), 4H-SiC by ion implantation of both the channel and source and drain ohmic contact regions. They formed the channel region and source and drain regions by doing two separate room temperature nitrogen ion implantations in box profile

to a depth of 0.3  $\mu\text{m}$ , with a projected volumetric concentration of  $6 \times 10^{17} \text{ cm}^{-3}$  for the channel and  $2 \times 10^{19} \text{ cm}^{-3}$  for the source/drain regions. The samples were then annealed at 1450  $^{\circ}\text{C}$  for 15 minutes with AlN cap to protect the sample surface during annealing, preventing Si from desorbing from the device surface. The source and drain ohmic contacts were formed by e-beam evaporation and lift-off Ni with a thickness of 100 nm, followed by 1200  $^{\circ}\text{C}$  3-minute annealing in vacuum. The 100 nm gate metallization was done with e-beam evaporation of Al.

In their DLTS measurements, the authors applied a  $-10 \text{ V}$  reverse bias to the Schottky gate to push the depletion region close to the N-implanted channel-SI substrate interface. Using rate windows ranging from 20.48 ms to 2.03 s, they observed several traps at the channel-substrate interface in relatively high concentrations of  $N_t = 0.01N_s$ , with  $N_s$  being the net carrier concentration. Figure 1.17 (a) and (b) show respectively the DLTS spectrum at a rate window of  $t_w = 20.48 \text{ ms}$  and the corresponding Arrhenius plots for the traps detected by the authors in the MESFETs. They indicate that the trap located at  $E_V + 0.5 \text{ eV}$  ( $P1'$ ) could be attributed to a point defect created by nitrogen implantation and the trap at  $E_V + 0.6 \text{ eV}$  ( $P2'$ ) could be related to the deep acceptor level introduced by the vanadium (V) dopant in the SI substrate. The authors, however, note that V usually has deep donor level at about  $E_V + 1.6 \text{ eV}$  and no such level was detected in their study. They attribute this to the fact that, their DLTS system specification sets 600 K as the upper limit of the temperature scan, which restricts the deep level detection limit to about 1 eV from the band edges. They point out that the origins of the other trap levels at  $E_V + 0.68 \text{ eV}$  ( $P3'$ ),  $E_V + 0.768 \text{ eV}$  ( $P4'$ ), and  $E_V + 0.89 \text{ eV}$  ( $P5'$ ) are unknown.

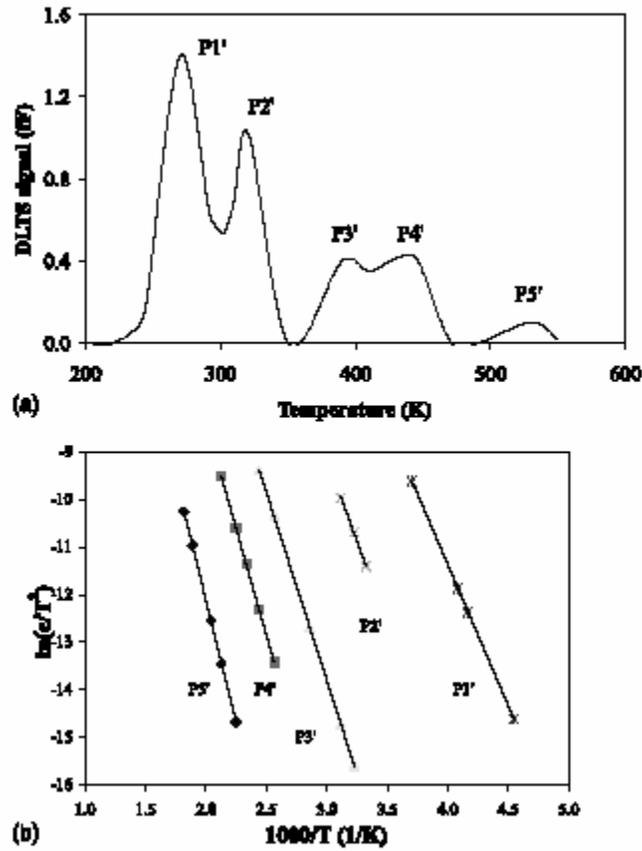


Figure 1.17: (a) DLTS signal and (b) Arrhenius plots of the channel-substrate interface traps detected by Mitra et al. in the 4H-SiC MESFET [10].

Figure 1.18 shows the variation of the P1' trap density across the channel-substrate interface obtained by the authors. They note that the trap density monotonically increases from the channel surface and inside the bulk substrate towards the channel-substrate interface. They further note that these traps, which are at the implanted region-substrate interface, strongly influence the channel carrier mobility. They observe that most of these traps fall under the residual implant lattice damage or implant-defect complexes category.

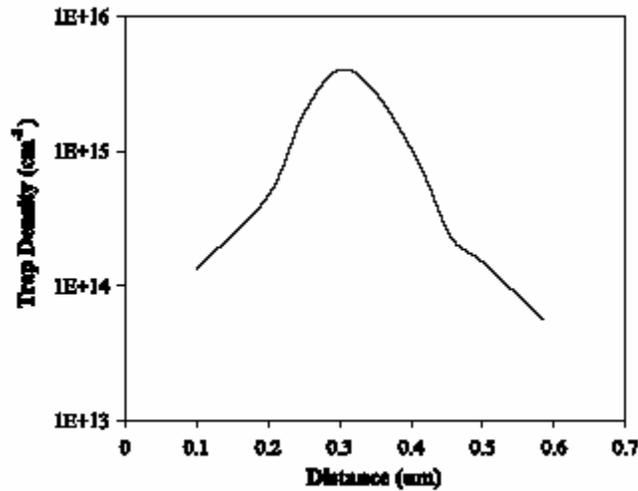


Figure 1.18: Variation of trap density across the channel-substrate interface for trap P1' ( $E_V + 0.51$  eV) in 4H-SiC MESFET obtained by Mitra et al. [10].

The authors observe from Figure 1.18 that after post-implant annealing, the majority of un-repaired lattice damage exists at the implant region-substrate interface. They further point out that residual lattice damage at the interface can be in the form of dislocation loops even for low implant doses. They go on to say that these dislocations may not exist in the as-implanted material but can be generated during annealing due to the coalescing of point defects at the implant region-substrate interface because of the stress at that region. Furthermore, the authors observe, the residual implant lattice damage can be greater for room temperature implantations than for elevated temperature implantations. They recommend that elevated temperatures implantations (500 °C and higher) and high temperature annealing should be done to minimize residual implant lattice damage in SiC. They further recommend that an optimized implantation and annealing temperature is required to achieve a higher mobility value and improved device behavior.

### **1.3.8. S. Mitra et al.: Deep-level transient spectroscopy study on double implant n<sup>+</sup>-p and p<sup>+</sup>-n 4H-SiC diodes [11]**

S. Mitra et al. also fabricated n<sup>+</sup>-p and p<sup>+</sup>-n junction diodes in n-type or p-type 4H-SiC epitaxial layers with doping concentration of about  $4 \times 10^{15} \text{ cm}^{-3}$  grown on the Si-face, 8° off axis, n<sup>+</sup>- or p<sup>+</sup>-4H-SiC substrates, respectively. Deep n- or p-type regions were created by selective-area, multiple-energy, box-profile nitrogen (or phosphorus) or boron (or aluminum) ion implantations, respectively. These were followed by shallow p<sup>+</sup> or n<sup>+</sup> regions formed, similarly by selective-area, multiple-energy, box-profile implants of Al or N, respectively. Single energy, shallow implants yielding  $2 \times 10^{19} \text{ cm}^{-3}$  N or  $1 \times 10^{20} \text{ cm}^{-3}$  Al was performed for both n- and p-type regions, respectively, for reliable ohmic contacts in the areas where planar ohmic contacts were placed. The authors performed all implants at 700°C using 2.5 μm thick SiO<sub>2</sub> layer as implant mask. The diodes were annealed at 1600-1650 °C for 10 minutes using AlN encapsulant as protective cap. The ohmic contacts were formed by e-beam evaporation of Ni on n-type regions and Ti/Al on p-type regions and alloyed at 1200°C for 3 min in a vacuum system. Figure 1.19 shows the structure of the p<sup>+</sup>-n junction diode used by the authors in their study. The structure of the n<sup>+</sup>-p device is similar with n-layers in place of p-layers and p-layers replacing n-layers.

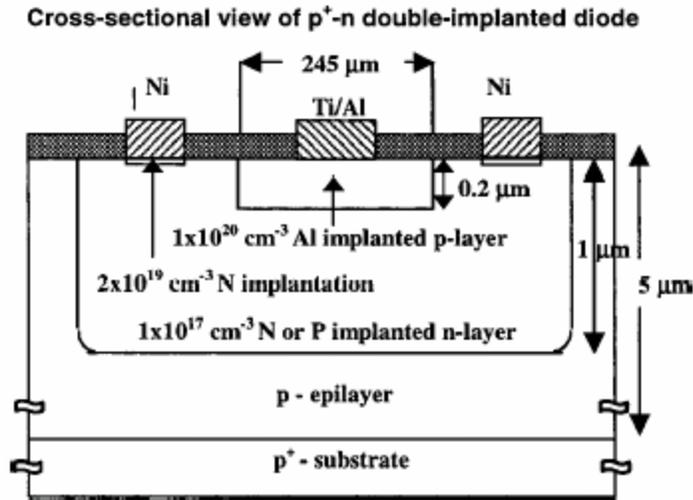


Figure 1.19: Cross-section of p<sup>+</sup>-n double implanted junction diode fabricated by the authors for their study [11].

In Figure 1.20 (a) and (b) is shown a typical DLTS spectrum and corresponding Arrhenius plots for the N/Al dual-implanted diodes respectively. The DLTS measurements were made with a 20 V reverse bias, a forward filling pulse of 1 V, and a rate window of 20.48 ms. The authors point out that the hump in the low temperature range (220-280 K) could be due to two poorly resolved deep centers. Using a different rate window of 2.03 s and 2 V pulse voltage, the authors observed two distinct defect levels, as shown in the inset, made up of one acceptor level at  $E_V + 0.28$  eV (N1Al) and one donor level at  $E_C - 0.42$  eV (N2Al). They believe these defect levels to be introduced by the Al implants.

Mitra et al. believe that the trap located at  $E_V + 0.51$  eV (N3Al) with capture cross section of  $6.5 \times 10^{-15}$  cm<sup>2</sup> is due to a complex, involving nitrogen and ion-induced defects. The authors point out that they have observed a peak with the same activation energy as that of the N3Al in fully nitrogen implanted MESFETs fabricated in bulk semi-insulating

4H-SiC [11]. They further state that the nitrogen involved in the N3AI center is the nitrogen dopant in the n-type epitaxial layer in which the  $n^+$ -p diode is formed and nitrogen in the tail of the  $n^+$  implanted layer. The authors observe that the trap N4AI located at  $E_V + 0.62$  eV could be attributed to the D center, which exhibits a deep acceptor behavior.

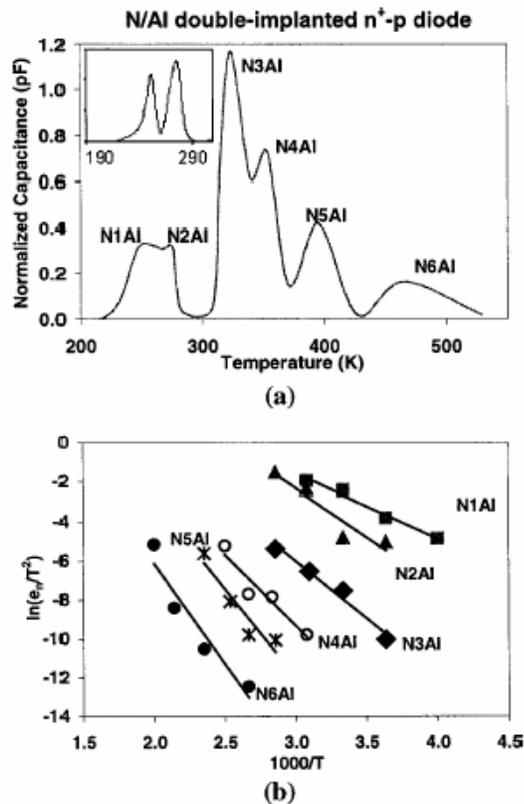


Figure 1.20: (a) Typical DLTS spectrum and (b) corresponding Arrhenius plots for N/Al double-implanted  $n^+$ -p diodes, fabricated by the authors [11].

Figure 1.21 represents a typical DLTS spectrum and corresponding Arrhenius plots obtained by the authors at a reverse bias of 20 V, a forward filling pulse of 1 V, and a rate window of 20.48 ms for  $n^+$ -p diodes with a deep boron-implanted p-region and nitrogen-implanted shallow  $n^+$ -region. They point out the presence of two dominant trap

signatures, N3B and N4B, of which the N3B has the same activation energy and capture cross-section as observed above in Figure 1.20(a) (N3Al and N4Al), which they attribute to a dopant-defect complex involving nitrogen.

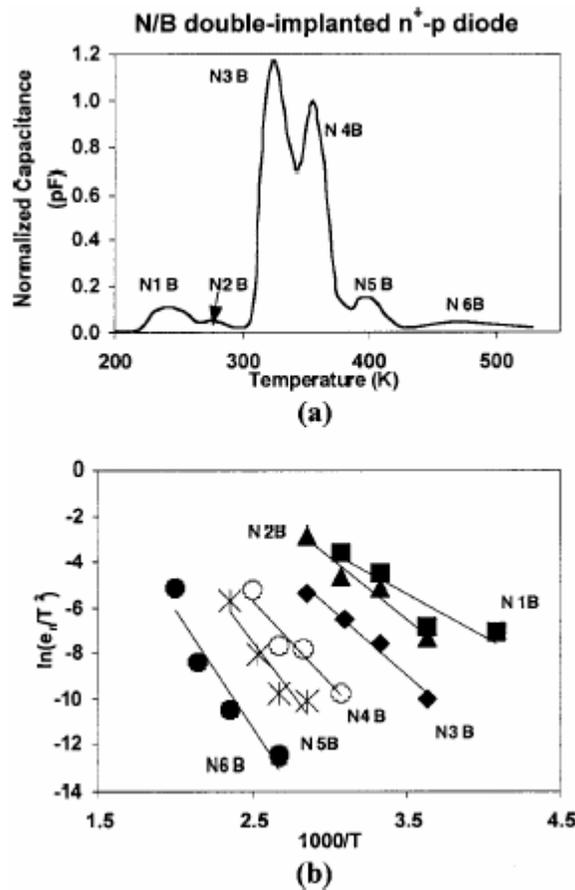


Figure 1.21: (a) Typical DLTS spectrum and (b) corresponding Arrhenius plot for N/B double-implanted n<sup>+</sup>-p diodes fabricated by the authors and used in their study [11].

Figure 1.22 shows that the intensity of the N3Al/N3B trap decreases as the reverse bias voltage increases, the authors point out. They explain that this means the trap concentration increases as the n<sup>+</sup>/p metallurgical junction is approached, indicating that this region has a higher defect concentration than the regions far away from the junction.

They point out that this suggests that the origin of the N3Al/N3B trap involves ion-induced defects.

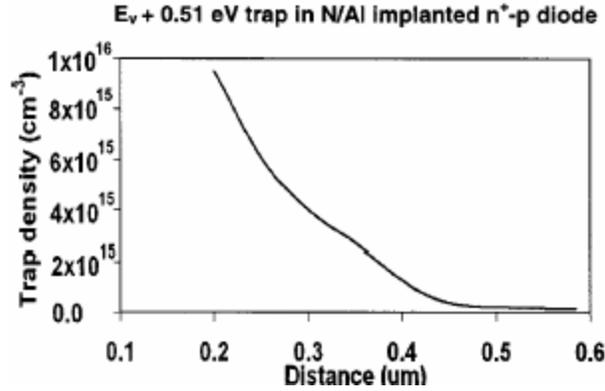


Figure 1.22: Defect-concentration-junction-depth profile for N3Al peak in N/Al double-implanted  $n^+$ -p diodes. The authors observe that the highest trap concentration occurs near the physical junction [11].

For the  $p^+$ -n diodes, the authors used a relatively low reverse bias voltage of approximately  $-4$  V for the DLTS measurements compared to the  $n^+$ -p diodes to avoid high leakage currents. Figure 1.23 depicts a typical DLTS spectrum and the corresponding Arrhenius plots measured by the authors for the diodes made with a deep N-implanted n-type region and a shallow Al-implanted  $p^+$ -region, for a forward filling pulse of 2 V and a rate window of 20.48 ms. They make the observation that, the trap center Al2N located at  $E_t - E_v = 0.27$  eV, which is an acceptor trap, and the center Al3N located at  $E_c - E_t = 0.43$  eV, which is donor trap, are more prominent and sharper than their respective peaks, N1Al and N2Al, in the DLTS spectrum of the N/Al  $n^+$ -p diodes shown in Figure 1.20(a). They point out that the trap concentrations are also about three orders of magnitude higher compared to the  $n^+$ -p diodes, which justify their assignment

of these peaks to the Al-related defects centers. They base this on the fact that the Al concentration in the  $p^+$ -region of the  $p^+$ -n diode is three orders of magnitude greater than the Al concentration in the p-region of the  $n^+$ -p diode.

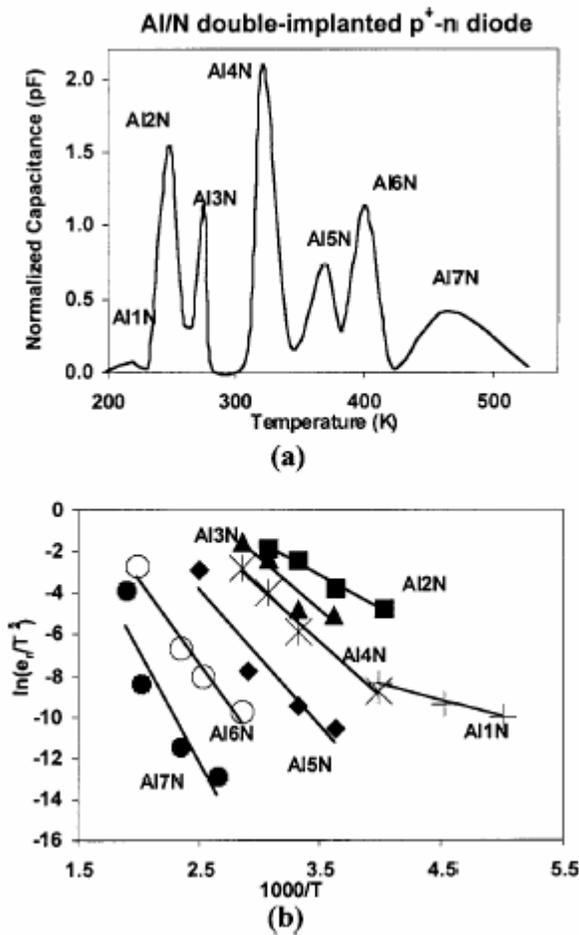


Figure 1.23: (a) Typical DLTS spectrum and (b) corresponding Arrhenius plot obtained by the authors for Al/N double-implanted  $p^+$ -n diodes [11].

In Figure 1.24 is shown a typical DLTS spectrum and corresponding Arrhenius plots for the  $p^+$ -n diodes made with phosphorus-implanted deep n-type region and Al-implanted shallow  $p^+$ -region, for a forward filling pulse of 2 V and a rate window of

20.48 ms. The authors observe that the trap centers Al2P and Al3P are respectively similar to the trap centers Al2N and Al3N in Figure 1.23 (a), which are assigned to Al-defect complex centers, since they have the same activation energy and cross section. Table 1.7 is a summary of the various traps observed by S. Mitra et al. and their possible origins.

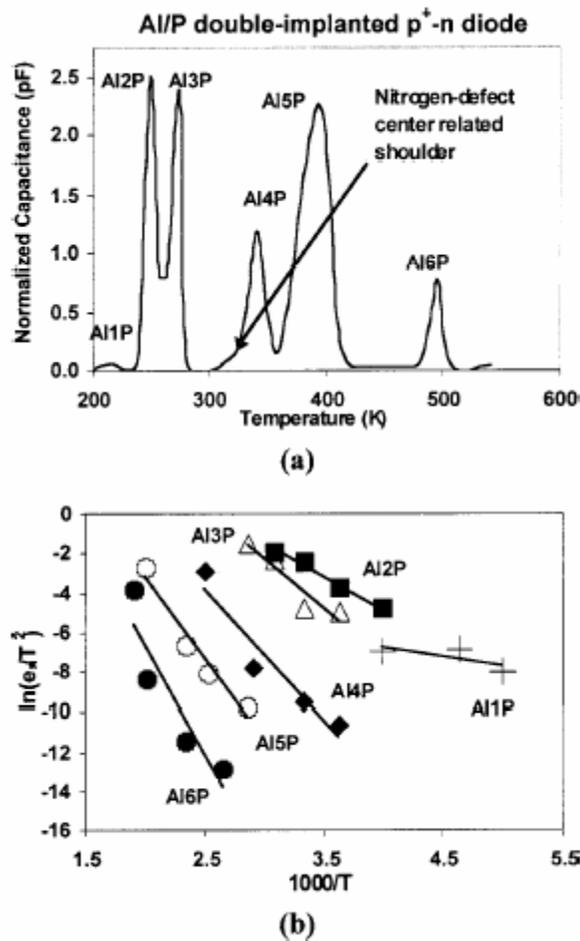


Figure 1.24: (a) Typical DLTS spectrum and (b) corresponding Arrhenius plot obtained by the authors for Al/P double-implanted p<sup>+</sup>-n diodes [11].

Table 1.7: Summary of traps observed by the authors in the double implanted junction diodes used in their study [11].

Trap	Peak location (eV)	Cross section (cm <sup>2</sup> )	Possible origin
N1Al, Al2N, Al2P	$E_F+0.27$	$7.0 \times 10^{-14}$	Al implantation
N2Al, Al3N, Al3P	$E_C-0.43$	$7.5 \times 10^{-14}$	Al implantation
N3Al, N3B, AlHN	$E_F+0.51$	$6.5 \times 10^{-15}$	Nitrogen-defect complex
N4Al, N4B, Al5N	$E_F+0.62$	$5.0 \times 10^{-14}$	D center
N5Al	$E_F+0.76$	$4-7 \times 10^{-14}$	Al-defect complex
NGAl, Al7N	$E_F+0.88$	$4-7 \times 10^{-14}$	Al-defect complex
N1B	$E_F+0.32$	$\sim 10^{-14}$	Not known
N2B	$E_C-0.46$	$\sim 10^{-14}$	Not known
AlHN	$E_C-0.15$	$5 \times 10^{-15}$	Nitrogen at C-site defect complex
Al6N	$E_F+0.78$	$6.0 \times 10^{-17}$	Vacancy-related intrinsic defect
AlHP	$E_F+0.08$	$3.4 \times 10^{-16}$	Not known
AlP	$E_F+0.6$	$1.4 \times 10^{-15}$	Phosphorus-defect complex
AlSP	$E_F+0.7$	$1.6 \times 10^{-15}$	Phosphorus-defect complex
A6P	$E_F+0.92$	$9 \times 10^{-15}$	Not known

In a SiC substrate implanted with the usual dopant atoms which control the electrical conductivity of the material, the inclusion of the dopant atoms in the SiC crystal lattice generate defects with energy levels in the band gap of the semiconductor material. In fact, any foreign atom irrespective of how it is incorporated into the semiconductor lattice structure (either by epitaxy, diffusion or implantation), intentional or unintentional constitutes a defect with an energy level in the semiconductor band gap. The energy levels of the usual dopants are close to the majority carrier band edges (conduction band or valence band) and are therefore termed shallow-level dopants or impurities. For SiC the usual shallow level dopants are nitrogen (N) and phosphorous (P) for n-type conductivity and aluminum (Al) and boron (B) for p-type conductivity. The energy levels (activation or ionization energies) of the shallow impurities are concentration dependent. The higher the concentration the closer the levels are to the majority carrier band edges.

For example, Capano et al. [27] put the activation energy of N in 4H-SiC at ( $E_C - 0.042$  eV) and ( $E_C - 0.084$  eV) for the hexagonal and cubic lattice sites respectively at a N concentration of  $2.3 \times 10^{17} \text{ cm}^{-3}$ , and the activation energy of P in 4H-SiC at ( $E_C - 0.058$  eV) and ( $E_C - 0.093$  eV) for the hexagonal and cubic sites respectively at P concentration of  $4.0 \times 10^{17} \text{ cm}^{-3}$ . It can be noted here that nitrogen occupies carbon lattice sites and phosphorous occupies silicon sites. Smith et al. [6] measured the activation energy of N in 4H-SiC at ( $E_C - 0.050$  eV) and ( $E_C - 0.105$  eV) for the hexagonal and cubic sites respectively. Ewvaraye et al. [28] determined the activation energy of B in 6H-SiC at the hexagonal (h) site to be ( $E_V + 0.27$  eV), and ( $E_V + 0.31$  eV) and ( $E_V + 0.38$  eV) for the two cubic sites ( $k_1, k_2$ ) respectively at B concentration of  $2 \times 10^{17} \text{ cm}^{-3}$ .

For implanted materials, in addition to the energy levels of the implanted impurities, the implantation-induced lattice damage caused by the bombardment of the semiconductor crystal lattice with the high-energy implant species results in defects with energy levels in the band gap of the semiconductor, as already pointed out above. For wide band gap semiconductors such as SiC, some of the implant damage induced traps can be very deep in the band gap. Implant damage induced traps can be created by irradiation with any high-energy particles, such as  $H^+$ ,  $He^+$ , electrons, and neutrons.

Several other authors have conducted various ion implantations and high-energy particle irradiations on SiC samples and have detected deep defect centers generated by the implantation or irradiation process. Frank et al. [29] implanted n-type 6H-SiC epitaxial layers on n-type substrate with  $He^+$  and observed the  $E_1/E_2$ ,  $Z_1/Z_2$ , and  $RD_5$  centers using DLTS as observed by Dalibor et al [8]. The samples were annealed at 1000

°C for 30 minutes. After 1400 °C anneal for 30 minutes the  $Z_1/Z_2$  disappeared. Using low temperature photoluminescence (LTPL), they observed that along with the nitrogen-related PL lines  $P_0$ ,  $R_0$ , and  $S_0$  and the titanium-related lines  $A_0$  and  $A_{90}$  there were three other LTPL peaks  $L_1$ ,  $L_2$ , and  $L_3$ , which they assigned to the  $D_1$  defect center observed in PL studies. In addition they observed a sharp LTPL peak at a wavelength position of 4349 Å. Correlating corresponding peak heights (i.e. defect concentrations) in DLTS to those in the LTPL spectra as a function of implanted  $He^+$  dose and annealing temperature, the authors conclude that the  $E_1/E_2$  in the DLTS spectra and the  $D_1$  center ( $L_1$ ,  $L_2$ ,  $L_3$ ) observed in LTPL spectra are caused by the same defect center. They further conclude that the  $Z_1/Z_2$  center and the center responsible for the 4349 Å LTPL line are identical, and caused by the same defect center. Frank et al. further conclude that the  $Z_1/Z_2$  center in 4H-SiC must be associated with the  $D_1$  center observed in LTPL and that the  $E_1/E_2$  center in 6H-SiC should also be associated with the  $D_1$  center as already indicated. Finally, they are of the opinion that the  $Z_1/Z_2$  in 4H-SiC corresponds to the  $E_1/E_2$  in 6H-SiC, and that the  $Z_1/Z_2$  in 6H-SiC is a different center associated with the LTPL line at 4349 Å. They further observe that this correlation is in agreement with the negative-U properties of the  $Z_1/Z_2$  (4H-SiC) and  $E_1/E_2$  (6H-SiC) defect centers.

Kawasuso et al. [30] detected irradiation-induced vacancy defects in high-quality n-type 4H- and 6H-SiC epilayers after irradiating the samples with 2 MeV electron beams and annealing in two steps below 700 °C and above 1200 °C, using positron annihilation and DLTS. The electron doses were  $1 \times 10^{15} \text{ cm}^{-2}$  and  $3 \times 10^{17} \text{ cm}^{-2}$  for the DLTS and positron annihilation measurements respectively, with the irradiation being

performed at room temperature. From the correlation between positron annihilation and DLTS data through annealing they confirmed that the  $E_1/E_2$  center in 6H-SiC and the  $Z_1/Z_2$  center in 4H-SiC, which exhibit negative-U properties, are caused by defect complexes including silicon vacancies.

According to Watkins et al. [31] and as reported by Hemmingsson et al. [32], a defect center possesses what is called a negative-U property if the center has the property of increasing the binding energy of carriers when capturing additional carriers. Hemmingsson et al. further state that the phenomenon occurs when the gain of total energy of the defect system overcomes the coulombic repulsion of the additional carriers. The gain in net attractive energy is supplied by a local rearrangement of the lattice and/or by the lattice itself, they assert. The negative-U centers,  $E_1/E_2$  (6H-SiC) and  $Z_1/Z_2$  (4H-SiC), are generated by electron irradiation and ion-implantation as already indicated above and have been determined to be acceptor-like with activation energies in the upper half of the 4H and 6H-SiC band gap irrespective of polytype [8], [33].

Nagesh et al. [34] used DLTS and resistivity measurements to characterize defects in as-grown and neutron irradiated epitaxially grown 3C-SiC (14-16  $\mu\text{m}$  thickness) on Si (100) substrates. From their experimental results, Nagesh et al. concluded that, the thick epilayers were free of deep level defects in the upper third of band gap, however, they noted that further studies were required to probe the lower two-thirds of the band gap. The authors further concluded that, in addition to an electron trap with activation energy of 0.49 eV, other neutron irradiation induced defects were detected with most of them confined to the lower two-thirds of the band gap. About 90% of the neutron induced

defects were removed by annealing at 350 °C, which they believe is significant, since it implies 3C-SiC devices (Schottky diodes in their experiments) can be operated at high temperatures even in a radiation-rich environment since any irradiation induced defects will anneal out at high operating temperatures.

Patrick et al. [23] introduced radiation defects into 6H-SiC by He<sup>+</sup>-implantation ( $5 \times 10^{14} \text{ cm}^{-2}$  at 150 keV) and electron bombardment ( $6 \times 10^{17} \text{ cm}^{-2}$  at 1 MeV). The authors observed a new low-temperature luminescence, produced by the defects, which is independent of the implanted species. One portion of the LTPL spectrum, the D<sub>1</sub> spectrum remains after 1700°C anneal. They identified two types of defects responsible for the LTPL spectrum and modeled them as (1) an impurity-defect complex with the most probable center being an impurity-vacancy pair, and (2) a pure-defect complex with the most likely candidate being a nearest-neighbor divacancy (i.e. vacancy-vacancy complex on adjacent sites). The authors consider the D<sub>1</sub> center to be possibly modeled by a C-Si nearest neighbor divacancy. In 6H-SiC the D<sub>1</sub> center is repeated three times (L<sub>1</sub>, L<sub>2</sub>, L<sub>3</sub> at 1.4 K and H<sub>1</sub>, H<sub>2</sub>, H<sub>3</sub> at 77 K) due to the three in-equivalent lattice sites of the 6H polytype. The two types of defect centers are present in both ion-implanted and electron-bombarded samples annealed at the same temperature (1300 °C) and taken from the crystal-growth furnace run. The major difference is that the D<sub>1</sub> spectrum has much greater strength in the ion-implanted sample. In the LTPL spectrum of an electron-bombarded sample taken at 1.4 K after 1300°C anneal taken by the authors, the D<sub>1</sub> spectrum is present but does not stand out compared to the many impurity-defect lines. In contrast, impurity-defect PL lines were faintly visible in the ion-implanted samples.

Patrick et al. observe that, a comparison of the  $D_1$  spectrum in ion- and electron-bombarded samples shows that its intensity depends strongly on defect concentration, since the heavier  $He^+$  ions generate higher  $D_1$  density, leading the authors to suggest that the  $D_1$  luminescence center is a pure-defect complex, possibly a divacancy as already noted. They observed the  $D_1$  center to have an unusual temperature dependence, with the low-temperature spectrum ( $L_1, L_2, L_3$  at 1.4 K) extinguished as the high-temperature spectrum ( $H_1, H_2, H_3$  at 77 K) is activated. At an intermediate temperature of 22 K both the low- and high-temperature forms are present. It should be noted that the  $D_1$  defect center corresponds to the  $E_1/E_2$  center in 6H-SiC and  $Z_1/Z_2$  center in 4H-SiC as already noted above.

From the above discussions, it is quite clear that ion implantation of semiconductors in general and silicon carbide in particular due to its compound nature results in crystal lattice damage, which generate traps in the semiconductor bandgap. These implanted induced lattice damage traps have to be taken into consideration in device design and operation. However, the possibility that implant induced lattice damage traps could lead to hysteresis in the I-V characteristics of semiconductor devices in general and MESFETs in particular have been overlooked in the literature, as already observed elsewhere in this work. It is quite plausible that implant induced lattice damage traps could generate hysteresis in the I-V curves of implanted devices.

## 1.4 Literature Review of Hysteresis in the Drain I-V Characteristics of MESFETs

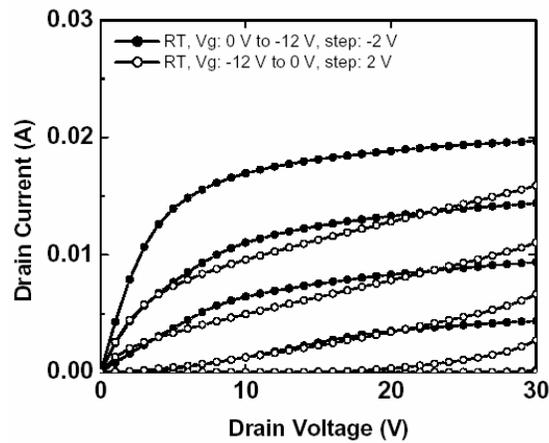
As already mentioned in this report, previous investigations into hysteresis in the drain I-V curves of MESFETs have mainly concentrated on semi-insulating substrate traps [14-22]. As a result hysteresis in the drain I-V characteristics of MESFETs and the related backgating effect have been largely attributed to semi-insulating substrate traps [14-22], even in implanted devices. The material that follows discusses a couple of references with regards to hysteresis in drain I-V characteristics.

### **1.4.1 A. P. Zhang et al.: Influence of 4H-SiC Semi-Insulating Substrates Purity on SiC Metal-Semiconductor Field-Effect Transistors Performance [15]**

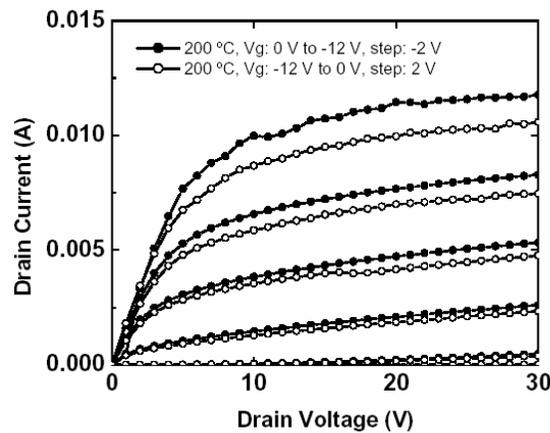
Zhang et al. compared the performance of two sets of 4H-SiC MESFETs fabricated on conventional Vanadium-doped semi-insulating substrates and Vanadium-free semi-insulating substrates with  $n^+$ -implanted source and drain ohmic contact regions. The device fabrication process includes mesa isolation, ohmic metal contact evaporation and annealing, recess gate etching, overlay metals, e-beam patterned T-shaped gate with 0.5  $\mu\text{m}$  footprint, and airbridge crossovers, but no surface passivation applied to the devices. Both types of devices have p-buffer layers between the channel and the semi-insulating substrates.

For both types of devices the drain I-V measurements were performed at room temperature (RT) and then at 200 °C. The drain-source voltage  $V_{DS}$  was varied from 0 V to 30 V as the gate-source  $V_{GS}$  was varied from 0 V to -12 V in steps of -2 V and then varied again from -12 V to 0 V in steps of 2 V. Figures 1. 25 (a) and (b) show the drain I-V characteristics of MESFET fabricated on the conventional Vanadium-doped semi-

insulating substrate at room temperature and 200 °C respectively. It can be seen in Figure 1.25 that the strong hysteresis effect at RT is significantly reduced at 200 °C due to thermal emission of electrons from trap centers at high temperatures. It should also be observed that the current levels at 200 °C are reduced relative to the levels at RT. This can be attributed to decrease in free electron mobility at high temperatures and the fact that this phenomenon dominates the drain current at high temperatures.



(a)

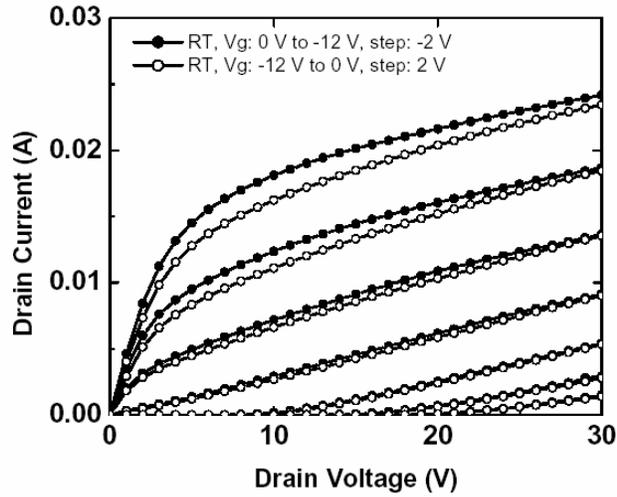


(b)

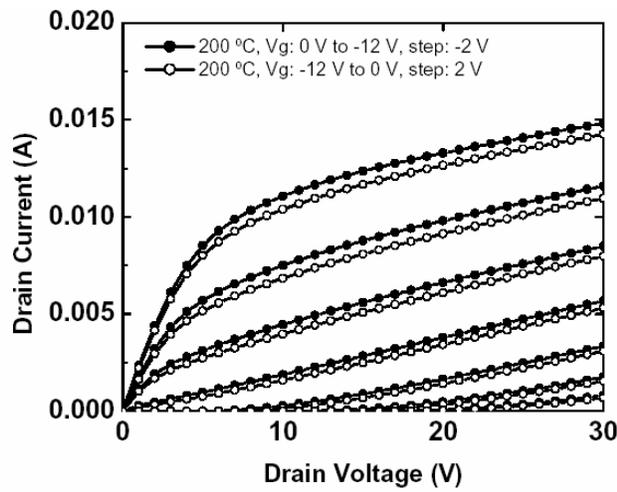
Figure 1.25: Drain I-V characteristics of 4H-SiC MESFET fabricated on conventional Vanadium-doped semi-insulation substrate at (a) room temperature (RT) and (b) 200 °C obtained by Zhang et al. [15].

Figures 1.26 (a) and (b) show respectively the drain I-V characteristics at room temperature and 200 °C of a 4H-SiC MESFET fabricated on Vanadium-free semi-insulating substrate. It can be observed that the hysteresis in the drain I-V curves at room temperature is significantly reduced relative to the room temperature I-V curves of the MESFET on the Vanadium-doped SI substrate in Figure 1.25(a), indicating the effectiveness of the Vanadium-free substrate. It should also be noted that there is no significant difference between the I-V curves at room temperature and 200 °C for the device on the Vanadium-free substrate, leading the authors to suggest that the traps responsible for the drain I-V hysteresis are not so temperature sensitive.

However, it is significant to observe that even with the Vanadium-free semi-insulating substrate hysteresis still persists in the drain I-V characteristics of the MESFET. And it should be remembered that the source and drain ohmic contact regions were implanted. While substrate traps could still be involved, it is possible that residual implant lattice damage traps could largely be responsible for the observed hysteresis in the drain I-V characteristics. This possibility is not addressed by the authors although it is well established in the literature that implant damage leaves several traps with energy levels distributed in the semiconductor bandgap [5-11, 24, 26]. Particularly, it is interesting and important to observe that the degree of hysteresis in the I-V curves of both types of MESFETs in Figures 1.25 and 1.26 respectively decreases with increasing negative  $V_{GS}$ . As will be shown in Chapter IV, simulations suggest that hysteresis due to or dominated by implant damage traps decreases with increasing negative  $V_{GS}$ .



(a)



(b)

Figure 1.26: Drain I-V characteristics of 4H-SiC MESFET fabricated on Vanadium-free semi-insulation substrate at (a) room temperature (RT) and (b) 200 °C obtained by Zhang et al. [15].

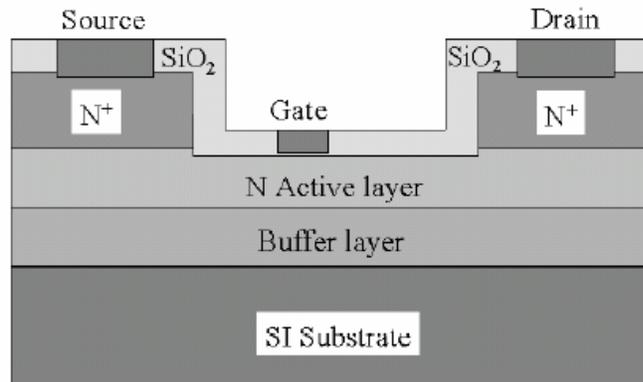
#### **1.4.2. Marc Rocchi: Status of the Surface and Bulk Parasitic Effects Limiting the Performance of GaAs IC's [17]**

Marc Rocchi performed experimental characterization of n-channel MESFETs used to fabricate GaAs IC's. Some of the MESFETs had p-buffer layers and the rest did not. Rocchi observed that the hysteresis in the drain I-V characteristics was drain voltage frequency dependent and peak drain voltage dependent. Similar results were obtained by Lo et al. [16] upon simulation of GaAs MESFETs fabricated on SI substrates. He attributes the hysteresis to trapping and detrapping processes that take place at the active layer-substrate interface for devices without buffer and buffer-substrate interface for devices with buffer. Rocchi further observed that MESFETs with p-buffer layer did not exhibit looping (hysteresis) in their drain I-V characteristics. This was not the case in the experimental devices used in this study. As already pointed out, both the devices without p-buffer and those with p-buffer exhibited hysteresis to about the same degree. It is therefore reasonable to look for a second mechanism, which could generate the observed hysteresis in the drain I-V curves of the MESFETs used in this project. Implant damage traps could be a possible source of the observed hysteresis.

#### **1.4.3. N. Sghaier et al.: Study of Trapping Phenomenon in 4H-SiC MESFETs: Dependence on Substrate Purity[14]**

Sghaier et al. investigated MESFETs fabricated on (1) Vanadium doped substrates grown by PVT sublimation technique and (2) Extremely low Vanadium content SI substrates grown by HTCVD. For all transistors, the authors performed drain

I-V measurements as a function of temperature. Figure 1.27 below shows the cross-section and parameters of MESFETs used in the study.



Gate length = 1  $\mu\text{m}$

Total gate width = 2x250  $\mu\text{m}$  for two-gate transistors

N<sup>+</sup> contact layer thickness = 0.2  $\mu\text{m}$ ; Doping concentration,  $N_D = 1 \times 10^{19} \text{ cm}^{-3}$

N-type active layer thickness = 0.3–0.4  $\mu\text{m}$ ;  $N_D = 1\text{--}2 \times 10^{17} \text{ cm}^{-3}$

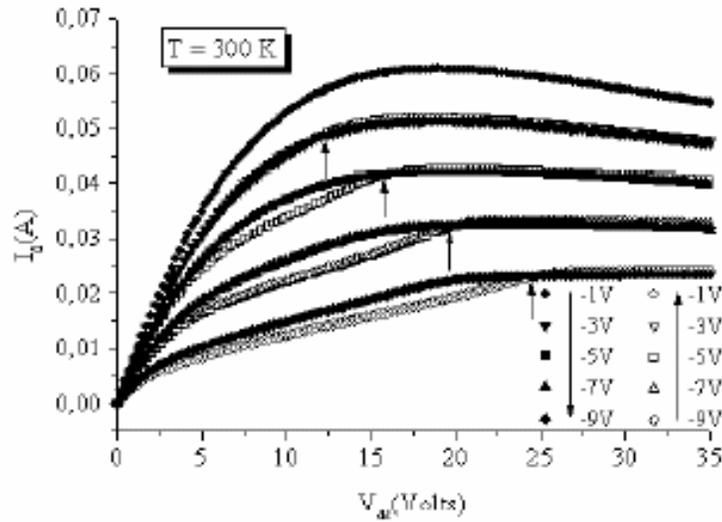
P-type buffer layer thickness = 0.3  $\mu\text{m}$ ;  $N_A = 1 \times 10^{16} \text{ cm}^{-3}$

Source-Gate Distance = 0.5  $\mu\text{m}$ ; Gate-Drain Distance = 2.0  $\mu\text{m}$

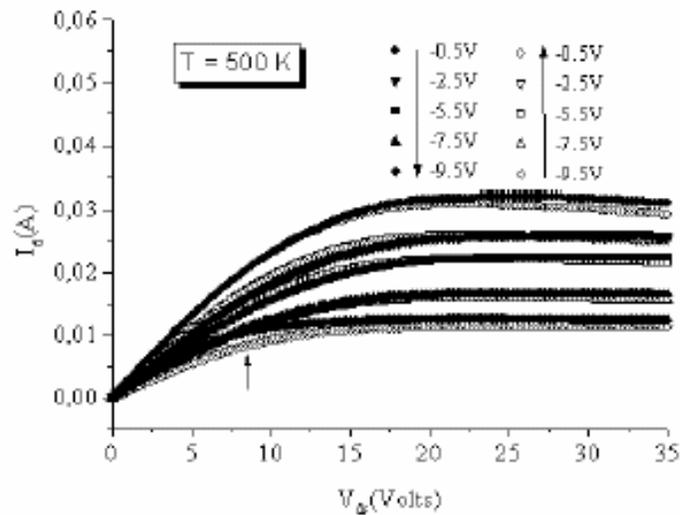
Figure 1.27: The structure and parameters of MESFETs used by Sghaier et al. in their study [14].

Figures 1.28 (a) and (b) show the drain I-V characteristics of a MESFET fabricated on V-doped PVT substrate at 300 K and 500 K respectively. In Figure 1.28(a) the solid symbols represent I-V measurements with increasing negative  $V_{GS}$  from  $-1 \text{ V}$  to  $-10 \text{ V}$  while the open symbols represent measurements decreasing negative  $V_{GS}$ . It can be seen from the figure that the hysteresis in the I-V curves increases for increasing negative  $V_{GS}$  due to increased injection of channel electrons into electron traps at

buffer/substrate interface, creating a parasitic backgate. In the I-V curves at 500 K in Figure 1.28(b) the solid symbols represent I-V measurements with increasing negative



(a)



(b)

Figure 1.28: Drain I-V curves for MESFET fabricated on V-doped PVT substrate at (a) 300 K and (b) 500 K measured by Sghaier et al. [14].

$V_{GS}$  from  $-5$  V to  $-9.5$  V and the open symbols represent measurements with decreasing negative  $V_{GS}$ . The authors note that the hysteresis decreases progressively as temperature increases and finally almost disappears at high temperatures such as 500 K due to thermal emission of electrons from traps.

The authors propose that the mechanism for the observed hysteresis is due to the presence of electron traps at the buffer/substrate interface. These electron traps can be deep neutral acceptors or ionized donors when empty. At high applied  $V_{DS}$  (30 V), the buffer layer/active layer p/n junction becomes highly reverse biased and the p-buffer layer can become fully depleted. Due to high E-field, electrons from the channel can be injected into the substrate resulting in a negatively charged depletion region in the substrate or buffer near the buffer/substrate interface. This depletion negative charge in turn induces a symmetrical depleted positive space charge region at the lower part of the channel at the channel/buffer interface, constricting the channel and therefore reducing the drain current as  $V_{DS}$  decreases. The negative space charge at the buffer/substrate interface acts as a parasitic gate which, is known in the literature as backgate, causing the drain current to decrease indirectly.

The authors are of the opinion that, their proposed hysteresis mechanism is consistent with increasing hysteresis effect as negative  $V_{GS}$  is increased, since for higher negative  $V_{GS}$ , the drain current flows close to the channel/buffer interface and is therefore more susceptible to parasitic backgating influence. The authors further assert that, increased current collapse and the hence

hysteresis should not be observed with increasing negative  $V_{GS}$  towards pinch off, if the traps were located at the upper surface of the active layer.

Figure 1.29 shows the drain I-V characteristics of a MESFET fabricated on HTCVD substrate and 300 K and 500 K.

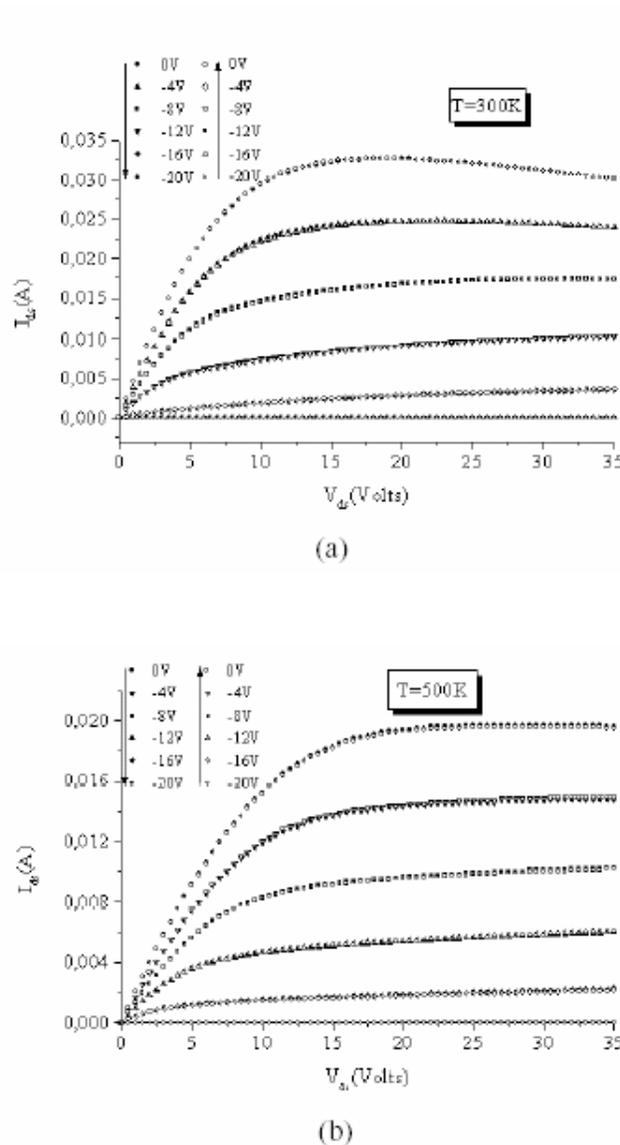


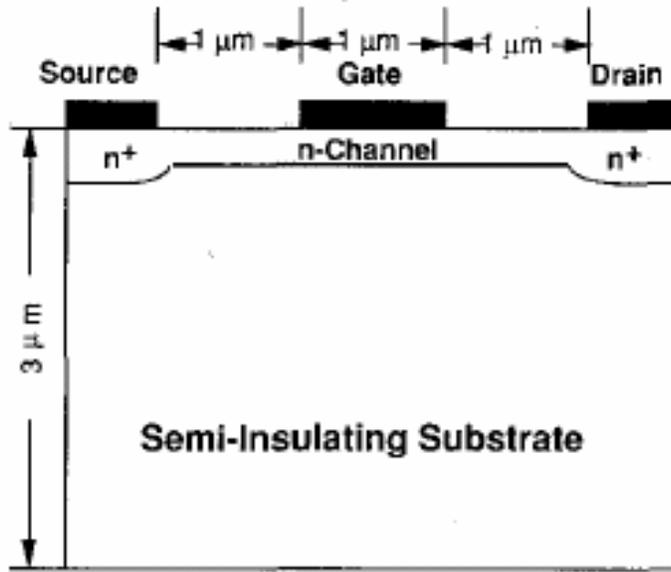
Figure 1.29: Drain I-V curves for a MESFET fabricated on HTCVD substrate at (a) 300 K and (b) 500 K measured by the Sghaier et al. [14].

Using Arrhenius analysis on data obtained from output (drain-source) conductance spectroscopy, the authors obtained activation energy of about  $E_C - 1.05$  eV for transistors fabricated on PVT SI substrates. This activation energy is close to the values reported by other authors for Vanadium acceptors [8, 12, 53, 55, 56, 57, 58, 60, and 66]. Based on their results, the authors believe that the main deep level observed in their experiment is related to the presence of Vanadium in the substrate.

#### **1.4.4. S. H. Lo et al.: Numerical Analysis of the Looping Effect in GaAs MESFETs [16]**

Lo et al. used two-dimensional numerical analysis (device simulation) to study the looping effect (hysteresis) in the drain I-V characteristics of GaAs MESFETs with SI substrates. They simulated both the transient and steady-state behaviors of the looping (hysteresis) phenomenon. The authors observed that the degree of hysteresis (looping) in the drain I-V characteristics is drain-source voltage frequency and peak drain-source voltage ( $V_{DS}$ ) dependent for a given gate-source voltage ( $V_{GS}$ ). They attribute the drain I-V loop to the difference in the distribution of ionized (empty) EL2 donor concentration in the substrate when  $V_{DS}$  rises and falls because of the trapping processes of the substrate EL2's. Figure 1.30 shows the structure and parameters of the simulation device.

For the simulations, gate voltage  $V_G$  varied from 0 V to the pinch-off voltage ( $V_{pinch-off}$ ) in steps of  $-0.2$  V, the source voltage  $V_S$  was set at 0 V, and the drain voltage  $V_D$  was a symmetric triangular wave with an amplitude of 2.5 V and frequency between 0.1 Hz and 1 kHz.



**Channel:**  $N_D = 1E17 \text{ cm}^{-3}$ , Depth =  $0.076 \text{ } \mu\text{m}$ .  
**Source/Drain:**  $N_D = 1.2E17 \text{ cm}^{-3}$ , Depth =  $0.1 \text{ } \mu\text{m}$ .  
**Substrate:** Shallow acceptor conc.,  $N_A = 1E15 \text{ cm}^{-3}$ .  
 EL2 concentration,  $N_T = 5E16 \text{ cm}^{-3}$ .  
 Metal-Semiconductor work function diff. =  $0.8 \text{ eV}$   
 $T = 300 \text{ K}$

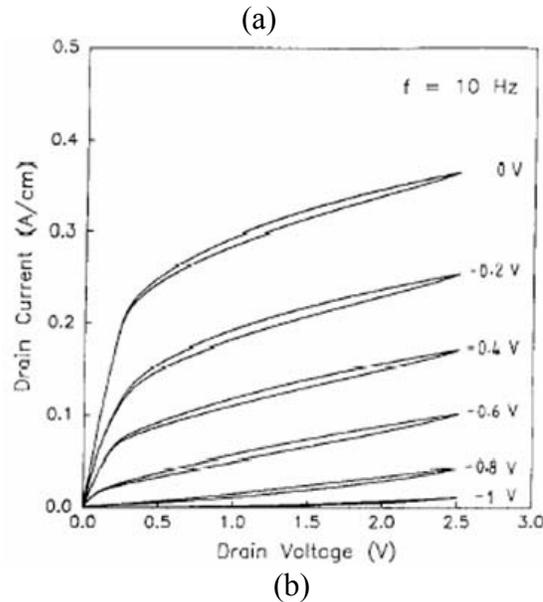


Figure 1.30: (a) The structure and parameters of the simulation device used by Lo et al. (b) Simulated drain I-V characteristics at  $f = 10 \text{ Hz}$  [16].

Figure 1.31 (a) and (b) show the conduction band edge along the center of the gate for drain-source voltage ( $V_{DS}$ ) frequency,  $f = 0.1$  Hz, 10 Hz, 1 kHz at  $V_{DS} = 0$  V and  $V_{DS} = 2.5$  V, respectively. The gate-source voltage  $V_{GS} = 0$  V for both cases. According to Lo et al. when the  $V_{DS}$  frequency,  $f$ , is between 1 Hz and 100 Hz, the period is close to time constant of the trapping process and the ionized (empty) EL2 distribution cannot reach a steady-state during the  $V_{DS}$  swings. Electron emission dominates at certain part of the  $V_{DS}$  swing and capture dominates at other part.

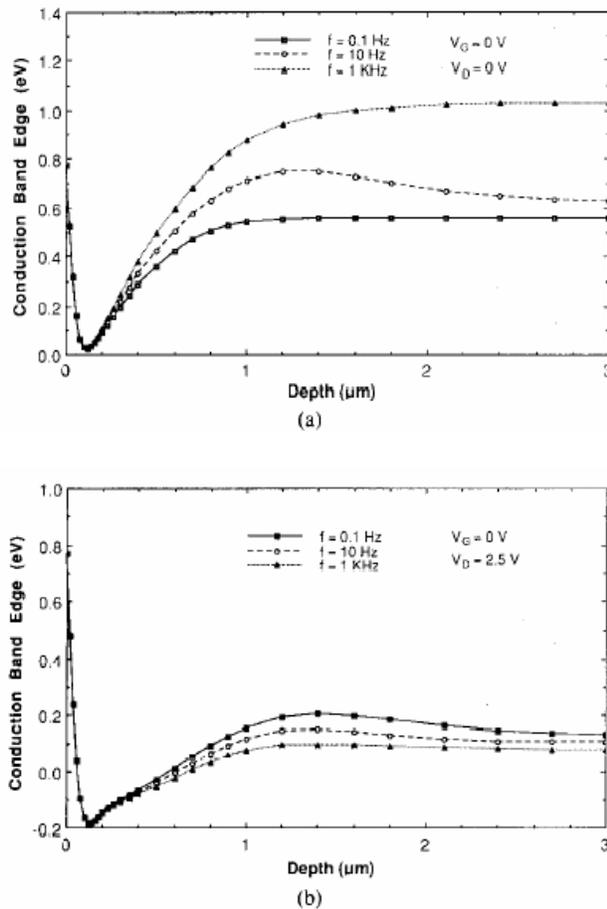


Figure 1.31: Depth profiles for the conduction band edge along the center of the gate at  $f = 0.1$  Hz, 10 Hz, and 1 kHz at (a)  $V_{DS} = 0$  V (b)  $V_{DS} = 2.5$  V obtained by Lo et al.  $V_{GS} = 0$  V [16].

The authors point out that when  $V_{DS} \sim 0$  V for  $f > 0.1$  Hz, potential barrier at the channel/substrate interface is higher than that at steady-state and the number of electrons injected into the substrate and trapped is small so electron emission is the dominant process. When  $V_{DS} \sim 2.5$  V for  $f > 0.1$  Hz, the barrier is lower than that at steady-state and electron capture is the dominant process. They further point out that as  $V_{DS}$  rises, the emission-dominant process gradually changes to a capture-dominant process, and as  $V_{DS}$  falls the capture-dominant process gradually changes to an emission-dominant process. At the end of the emission process the number of ionized (empty) EL2s in the substrate is larger and the edge of depletion region is closer to the channel/substrate interface. At the end of the capture process the number of ionized (empty) EL2s is less and, more electrons are captured, and the depletion region extends into the substrate. The difference in ionized (empty) EL2 distribution is shown in Figure 1.32(a) for  $V_{DS} = 1.5$  V, while the corresponding conduction band edge is shown in Figure 1.32(b).

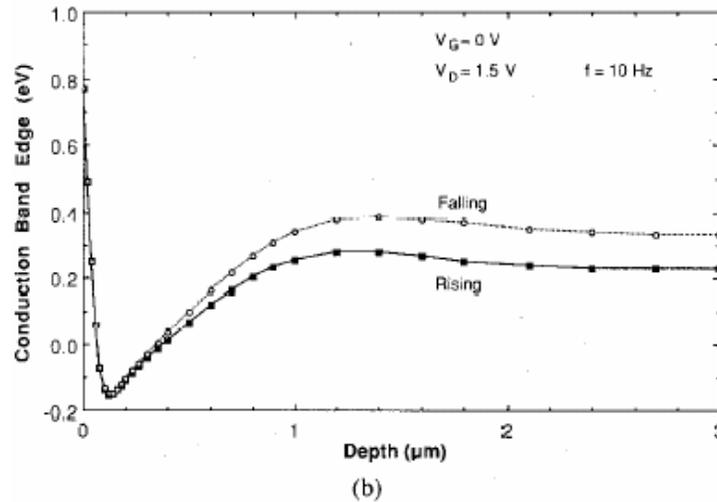
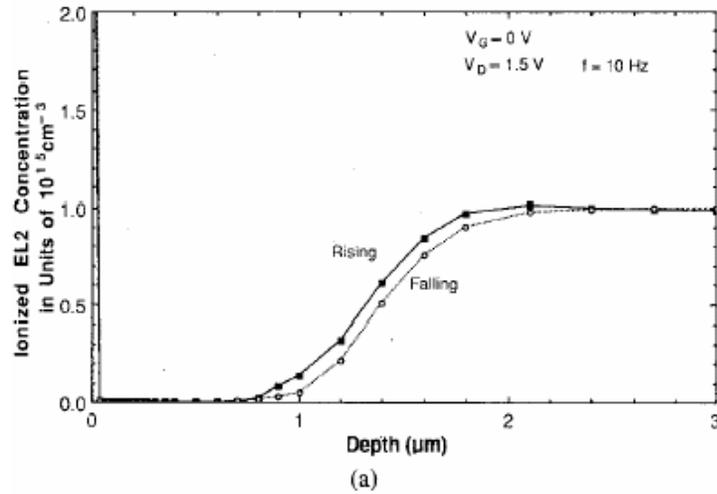


Figure 1.32: (a) Depth profiles of ionized (empty) EL2 concentration at  $V_{DS} = 1.5 \text{ V}$  when  $V_{DS}$  is rising and falling at  $f = 10 \text{ Hz}$  [16]. (b) Depth profiles of conduction band edge at  $V_{DS} = 1.5 \text{ V}$  when  $V_{DS}$  is rising and falling at  $f = 10 \text{ Hz}$  [16].

The authors further go on to say that when  $V_{DS}$  falls, due to the captured electrons during the capture-dominant phase, the interface potential barrier is higher and the free electron concentration in the substrate is lower than when  $V_{DS}$  rises. So when  $V_{DS}$  falls the depletion region is wider, the interface potential barrier is higher and the

resulting drain current is lower. When  $V_{DS}$  rises, the depletion region is narrower, the interface potential barrier is lower, and the drain current is higher. A loop (hysteresis) therefore appears in the drain I-V curves. Figure 1.33 shows the free electron concentration at  $V_{DS} = 1.5$  V as  $V_{DS}$  rises and falls.

Lo et al. explain the peak drain voltage dependence of the looping effect as follows. For small  $V_{DS}$  the number of electrons injected into the substrate is small. Thus for small peak  $V_{DS}$ , the distribution of ionized (empty) EL2s in the substrate side and hence the number of captured electrons is hardly influenced by the applied drain voltage. There is therefore no difference in trap occupation whether the drain voltage rises or falls and hysteresis does not appear in I-V characteristics.

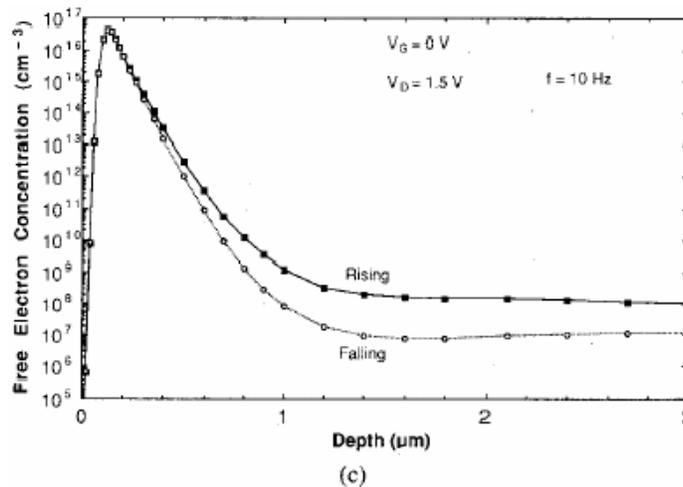


Figure 1.33: Free electron concentration at  $V_{DS} = 1.5$  V when  $V_{DS}$  is rising and falling obtained by Lo et al. [16].

### 1.4.5. I. Son et al.: Modeling Deep-Level Trap Effects in GaAs MESFETs[18]

Son et al. performed modeling and numerical simulations to investigate the effects of deep level traps on GaAs MESFET characteristics. They used four different transistors with various deep level trap (DLT) distributions. Figure 1.34(a) shows the structure and parameters of the MESFETs analyzed. For the simulation the authors applied a voltage pulse of sine function to the drain with a sweeping time (pulse width) of 1 ms and a peak voltage of 3 V. The simulations were performed at gate voltages of 0 V and  $-1$  V. Figure 1.35(a) shows the parameters of MESFETs used by Son et al. in their simulations and Figure 1.35(b) shows drain I-V curves for transistor TR1.

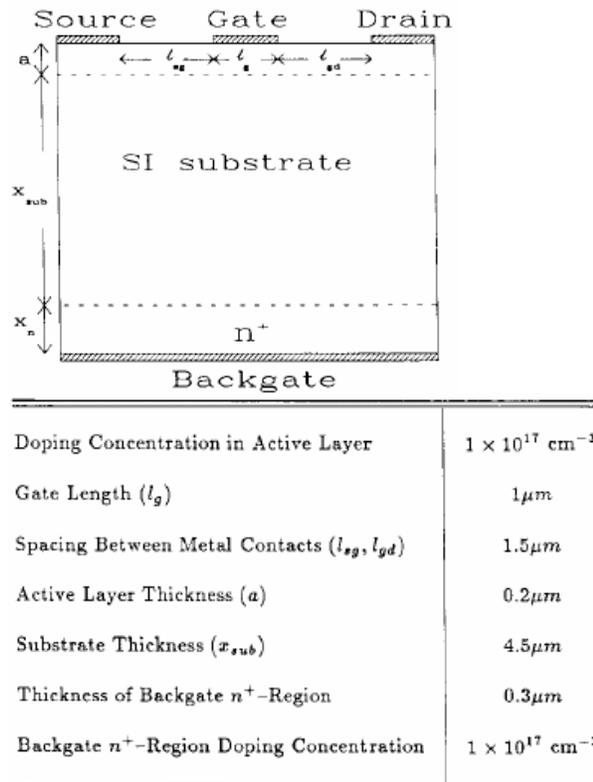
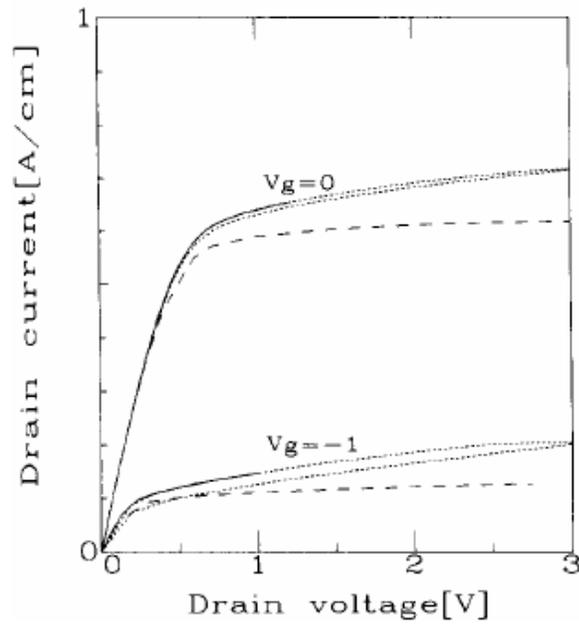


Figure 1.34: The structure and parameters of MESFETs used by Son et al. in their simulations [18].

Transistor	DLT Concentration ( $\text{cm}^{-3}$ )			Shallow Donor Impurity Concentration In Substrate ( $\text{cm}^{-3}$ )
	Surface ( $\text{cm}^{-2}$ )	Channel	Substrate	
TR1	$1 \times 10^{12}$	$1 \times 10^{16}$	$1 \times 10^{18}$	$1 \times 10^{14}$
TR2	$1 \times 10^{12}$	$1 \times 10^{16}$	$1 \times 10^{14}$	$1 \times 10^{12}$
TR3	$1 \times 10^{12}$	0	$1 \times 10^{18}$	$1 \times 10^{14}$
TR4	0	$1 \times 10^{16}$	$1 \times 10^{16}$	$1 \times 10^{14}$

(a)



(b)

Figure 1.35: (a) The parameters of MESFETs used by Son et al. in their simulations [18]. (b) Simulated drain I-V curves of transistor TR1 obtained by Son et al. [18].

Similar results were obtained for transistors TR3 and TR4. No hysteresis was observed for transistor TR2 due to low DLT concentration of  $1 \times 10^{14} \text{ cm}^{-3}$ . Since similar results were obtained for transistors TR1, TR3, and TR4, the authors conclude that the hysteresis is due to slow change of negative space charge in the substrate as  $V_{DS}$  rises and

falls due to trapping of channel electrons by substrate deep level traps. The authors also observed that hysteresis is a function of peak  $V_{DS}$  (solid curves) and no hysteresis occurs in steady-state (dashed curves).

### **1.5 Use of OAS to Detect Deep Level Implant Damage Traps**

Defect centers with energetically shallow levels in the semiconductor band gap and even energetically deep defect levels in the band gap of narrow band gap semiconductors, such as silicon, can be observed by the more traditional methods such as Hall effect, thermal admittance spectroscopy (TAS), standard (thermal) deep level transient spectroscopy (DLTS). For wide band gap semiconductors such as SiC, the study of defect centers with energetically deep defect levels deep in the band gap is more difficult because abnormally high temperatures are required to move the Fermi level close to mid-gap [35]. The idea here is to supply enough thermal energy to the semiconductor to make it more intrinsic and move the Fermi level to near the middle of the band gap. In this way, electron traps (neutral donors and ionized acceptors) in n-type materials with energy levels above the Fermi level can emit their electrons to the conduction band and be detected, and hole traps (neutral acceptors and ionized donors) in p-type material with their energy levels below the Fermi level can emit their holes to valence band (i.e. trap electrons from the valence band). Once the Fermi level is in the middle of the band gap (i.e. intrinsic level - mid gap), traps in the upper half of the band gap will emit their electrons to conduction band and traps in the lower half will emit their holes to the valence band. The electrons and holes move to the edge of the depletion

region where they are detected by the change in the capacitance and conductance [35]. According to Dalibor et al. [8], for wide band gap semiconductors such as SiC, the energy range in the band gap measured from the majority carrier band edge, which can be studied with standard (thermal) DLTS, is limited in most cases (depending on capture cross section) to about 1.3 eV. This limitation, they say, is due to the fact that majority carriers have to be thermally emitted from the trap level into the majority carrier band. Therefore depending on the particular SiC polytype, a certain energy range in the middle of the band cannot be probed with standard DLTS. It is conceivable that if a portion of the band gap cannot be probed by thermal DLTS, then that portion cannot also be probed by TAS, since both techniques use the same thermal excitation process to excite carriers from defect centers to the respective majority carrier band and both employ capacitance transient techniques. They conclude that the approachable energy range can be extended, if the charge carriers are optically excited. The optical excitation can be achieved through the use of such optical detection techniques as optical admittance spectroscopy (OAS) and optical DLTS (ODLTS). Thus for both admittance spectroscopy and deep level transient spectroscopy, carriers may be excited from defect centers with energy levels deep in SiC band gap by illuminating the material with monochromatic light of such a wavelength that the photon energy is equal to the transition energy from the defect center to the respective band edge [35].

In this study, as already pointed out, device simulation using the two-dimensional device simulator, Medici<sup>TM</sup> and optical admittance spectroscopy (OAS) are used to verify why hysteresis is observed in the drain I-V characteristics of both the MESFETs with and

without p-buffer layer to about the same degree but TAS, thermal DLTS, and thermal conductance spectroscopy (TCS) could detect the traps in the devices without the p-buffer layer but not in the devices with buffer. It is quite plausible that the energy level of the traps responsible for the hysteresis in the drain I-V curves of both types of devices is too deep in the 4H-SiC band gap to be detected by the particular equipment used for the thermal spectroscopic measurements. The principles of optical admittance spectroscopy (OAS) and OAS measurement results will be presented in Chapter V.

## CHAPTER II

### EXPERIMENTAL SETUP

The power MESFET devices used in the experimental characterization have gate length of about 0.5  $\mu\text{m}$  and total gate periphery that ranges from 0.2 mm to 22 mm [12]. The devices were fabricated on epitaxial structures which nominally consisted of a 0.3  $\mu\text{m}$  thick n-type active layer (channel) with net doping of  $2.5 \times 10^{17} \text{ cm}^{-3}$ , either grown directly on the semi-insulating (SI) substrate or grown on a 0.55  $\mu\text{m}$  thick p-type buffer layer with net doping less than  $5 \times 10^{15} \text{ cm}^{-3}$ , which separates the channel from the SI substrate. The p-buffer and n-channel were grown using chemical vapor deposition (CVD) on physical vapor transport (PVT)-grown semi-insulating (SI) substrates purchased from Cree Research, Inc., Durham, North Carolina. The source and drain regions of the devices were nitrogen ion-implanted to provide low-resistance ohmic contacts, and air bridges were used to interconnect the source fingers. The microphotograph of one of the devices with two gate fingers is shown in Figure 2.1 and Figure 2.2 exhibits the microphotograph of a MESFET with twelve gates.

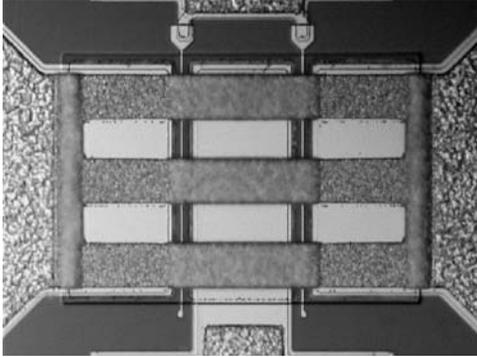


Figure 2.1: Microphotograph of a 4H-SiC MESFET with gate periphery of 0.2 mm with two gates used in the experimental characterization.

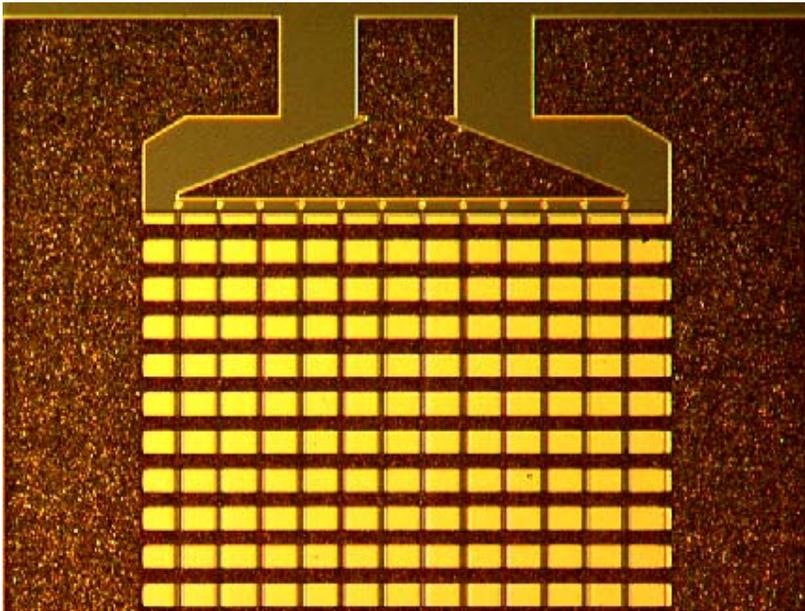


Figure 2.2: Microphotograph of a SiC MESFET with twelve gates.

The output DC characteristics, output thermal admittance spectroscopy (TAS), gate-source thermal conductance spectroscopy (TCS), and thermal deep level transient spectroscopy (DLTS) measurements of the devices were made on both packaged and unpackaged devices in the temperature range of 300-500 K. The DC characteristics were measured using Keithley 237 and Keithley 238 source-measure units (SMUs). The output thermal admittance spectroscopy, thermal gate-source conductance spectroscopy, and DLTS measurements were performed in an Advanced Research Systems DE-202 closed-cycle cryostat using an HP4274A precision LCR meter and HP4280A capacitance meter. The device package temperature was controlled within  $\pm 0.3$  K.

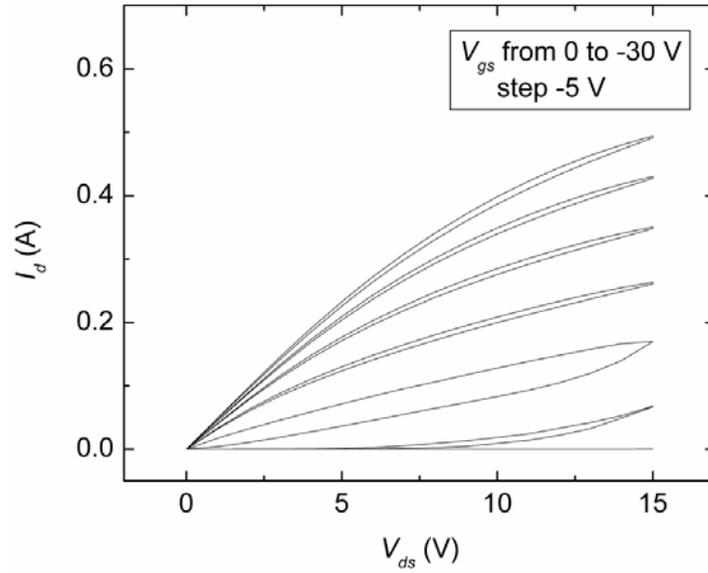
The optical admittance spectroscopy measurements were performed on two-gate MESFETs, as shown in Figure 2.1 above, with an HP4284A multi-frequency LCR meter operated in the high-resolution mode at 20 kHz. The measurements were first made at 300 K (room temperature) and then at 200 K. A 450-1000 W Oriel Instruments Xenon arc lamp, model 6269, and an Oriel Monochromator Model 74100 provided the monochromatic light. The DC bias was set at 0 V and the AC measuring signal amplitude was 0.05 V.

## CHAPTER III

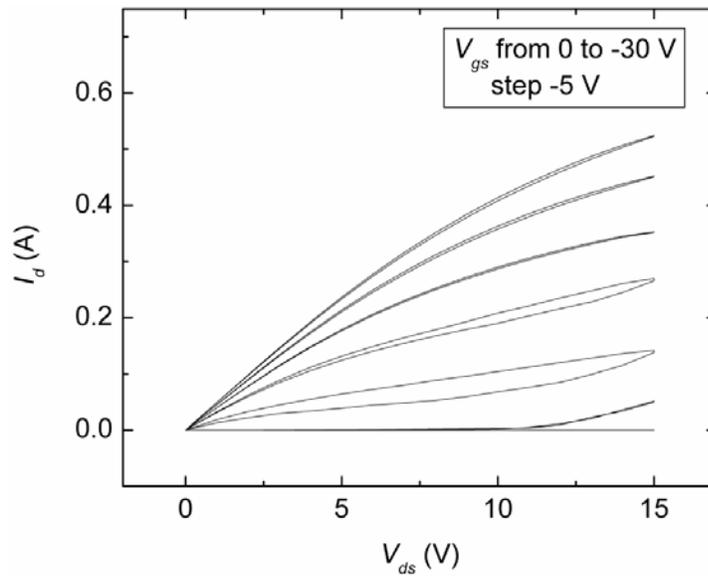
### EXPERIMENTAL DEVICE CHARACTERIZATION

#### 3.1 Results of Experimental Device Drain I-V Characterization

Figures 3.1 and 3.2 show typical drain I-V characteristics of MESFETs with and without p-buffer layer with total gate periphery of 1.2 mm at 300 K and 480 K respectively. The pulse period of  $V_{DS}$  used in the I-V measurements is about 15s, which results in a  $V_{DS}$  frequency of about 0.067Hz. As can be observed, the output characteristics of both types of devices show drain current instability, which is manifested as hysteresis in the drain I-V curves. At a particular temperature the characteristics of both types of devices with and without p-buffer are generally similar with both types of devices showing hysteresis in their I-V curves. For example, it can be seen from Figure 3.1 that the drain I-V curves at 300 K for a MESFET without buffer and one with buffer are generally similar although the magnitude of the hysteresis in the I-V curves of the device without p-buffer is slightly greater than that of the device with p-buffer. The hysteresis disappears completely in the temperature range of 450 K to 500 K at large negative gate voltages, as can be seen from Figure 3.2. At small gate voltages there is almost no difference in the degree of hysteresis at 300 K and a high temperature such as 480 K. These facts reveal that drain current instability at low and high gate voltages is controlled by impurities with different ionization time constants.



(a)



(b)

Figure 3.1: Typical drain I-V characteristics at  $T = 300$  K for (a) MESFET without p-buffer layer (b) MESFET with p-buffer layer.

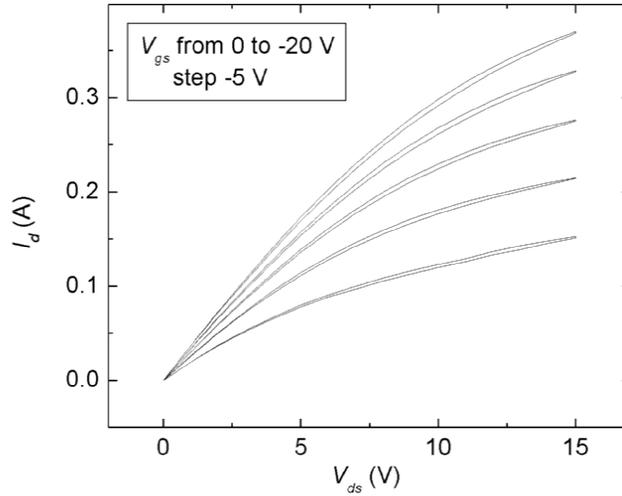


Figure 3.2: Typical drain I-V characteristics of both types of MESFETs at  $T = 480$  K

### 3.2 Results of Experimental Device Thermal Spectroscopic Characterization

Drain-source thermal admittance spectroscopy (TAS), gate-source thermal conductance spectroscopy, and gate-source thermal deep level transient spectroscopy (DLTS) measurements were made in the saturation regime to determine the parameters of the defect centers responsible for the drain I-V hysteresis. Here it should be noted that saturation is not well defined in these devices as exhibited by the drain I-V characteristics. The TAS measurements were done with drain-source voltage ( $V_{DS}$ ) of 15 V, gate-source voltage ( $V_{GS}$ ) of  $-15$  V and AC small signal voltage with amplitude of 1 V RMS. Figure 3.3 shows the output admittance phase angles of both types of devices.

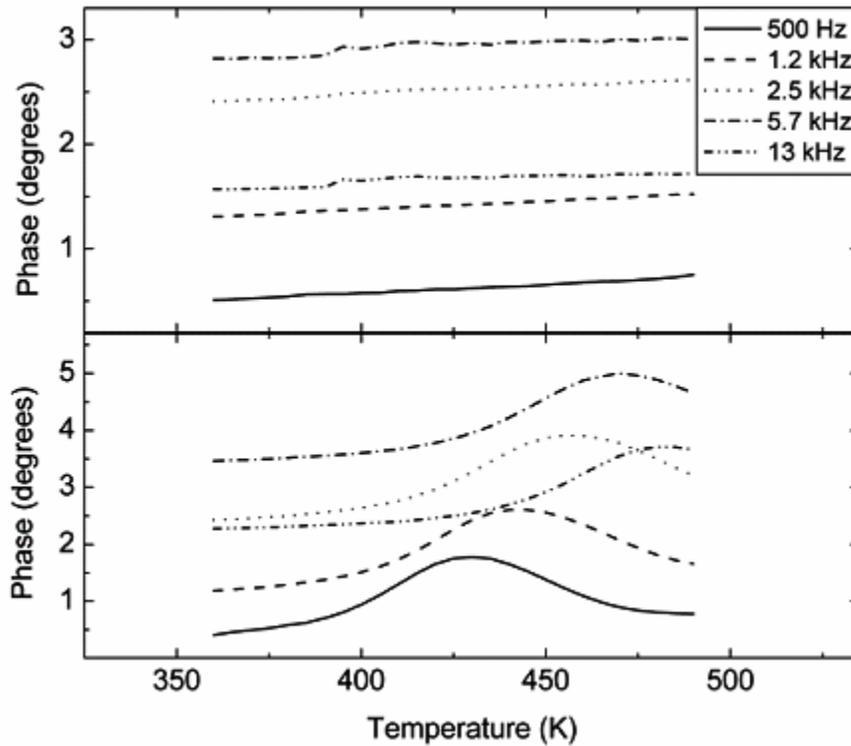


Figure 3.3: Drain-source thermal admittance phase angles as a function of temperature with the AC signal frequency as a parameter for (top) a MESFET with p-buffer layer and (bottom) a MESFET without p-buffer layer.

Admittance phase angle of the device with p-buffer layer is practically constant as temperature increases with no peaks and only modest frequency dependence. This shows there is practically no trapping and emission of carriers by traps in the SI substrate and therefore no changes in buffer-substrate depletion region width and hence no variation in junction capacitance. As a result, admittance phase angle remains constant. The low values of admittance phase for a given frequency indicate low parasitic capacitance over the measurement temperature range. On the other hand, the devices without p-buffer layer have an output admittance phase angle that peaks in a particular temperature range depending on the measurement frequency. This, suggest the presence of trapping and

emission processes and provides information on the time constant of the defect centers responsible for the frequency dispersion of the output admittance. In this case as temperature increases, maximum emission of trapped electrons occurs at the substrate side of the channel-substrate interface leading to minimum number of trapped electrons and hence minimum space charge due to trapped electrons in the substrate. This leads to a corresponding minimum space charge at the channel side of the channel-substrate interface and therefore minimum overall channel-substrate depletion layer width. This in turn leads to increased (maximum) channel-substrate depletion layer capacitance and increased (maximum) admittance phase. Thus the output admittance data demonstrate the degree of electrical isolation of channel electrons from the SI substrate traps provided by the low-doped p-buffer layer in the small-signal regime of operation. In both types of devices at a particular temperature, as frequency increases the trapping/emission rate cannot keep up with the signal. Therefore there is not enough time for carriers (electrons in this case) to be trapped and emission exceeds trapping. The number of trapped electrons decreases and as a result, the space-charge region width due to trapped electrons decreases, leading to increased depletion capacitance and hence admittance phase, as frequency increases.

In Figure 3.4 is presented Arrhenius plots calculated from output admittance, gate-source differential conductance, and transient capacitance spectroscopy data for devices without p-buffer layer. Gate contact measurements were done on completely pinched-off channel at a  $V_{GS}$  that ranges from -25 V to -30 V. At smaller gate voltages conductance peaks and capacitance transients disappeared, indicating that carrier trapping

takes place at the channel-substrate interface. Since gate contact measurements were done at relatively large reverse bias voltages, time constants extracted from the capacitance and conductance data were corrected for the Poole-Frenkel effect [64, 65]. All three measurement techniques gave similar values of activation energy of the impurity responsible for carrier trapping in the range  $0.95 \pm 0.04$  eV, if impurity capture cross-section  $\sigma$  is assumed to be independent of temperature, and  $1.02 \pm 0.04$  eV for  $\sigma \propto T^{-2}$ . These values correspond to vanadium acceptors [53-58, 60] and are consistent with the presence of vanadium in the semi-insulating substrate.

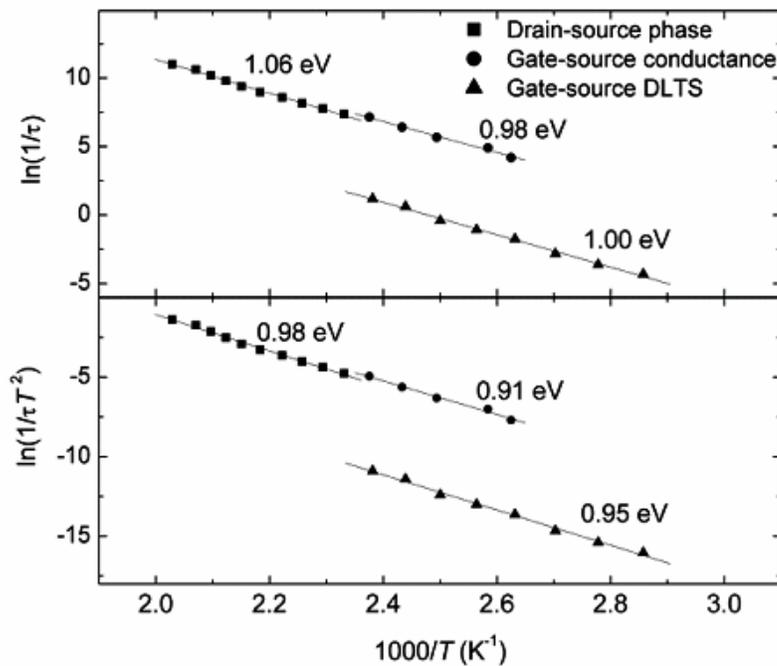


Figure 3.4: Arrhenius plots obtained from drain-source admittance, gate-source conductance, and gate-source DLTS for a MESFET without p-buffer for (top) the case of  $\sigma \propto T^{-2}$  and (bottom) the case of  $\sigma = \text{constant}$ .

As in the case of admittance measurements, conductance spectroscopy and DLTS measurements on the devices with p-buffer showed peak-free conductance and no capacitance transients. The measurements were performed with the same bias voltages, frequencies and temperatures as on the devices with no buffer. Measurements for device bias values varying in the range of  $\pm 5-7$  V, as well as for different measurement frequencies and time windows produced similar results. It can therefore be concluded that the low-doped buffer provides good electrical isolation of the device channel from the substrate in the device operating modes used in the measurements.

## CHAPTER IV

### DEVICE SIMULATION

#### 4.1 General Review of Device Simulation

In device simulation a computer program is used to determine the current and voltage distributions inside the device [38]. The current distribution is given by its magnitude and direction. The program determines the current and voltage distributions by dividing the device into small volumes (device discretisation) in which various device parameters are considered constant for each volume element [38, 39, 40]. Hence, there is one current vector, one potential, one set of concentration values (for electrons and holes), one set of mobility values ( $\mu_n$ ,  $\mu_p$ ) among others [38]. The simulation program then uses mathematical routines (numerical methods) to discretise the device equations over the volume elements [38, 39, 40]. The program uses finite differences in which the volume elements are cubes or finite elements in which the volume elements are arbitrarily shaped as the discretisation base [38, 39]. Since the discretisation into cubes is an easier process than discretisation into arbitrary shapes, finite differences are easier than finite elements, and are more often used [38]. The number of elements determine the accuracy of the solution, however, the greater the number of volume elements the longer the computer time and the larger computer memory required. The computation procedure is an iterative process, which involves matrices with device parameter values for all the

volume elements. Therefore the demands on computer resources increase rapidly as the number of volume elements increases [38, 39, 40].

Since a real device is three dimensional (3-D) in nature, a 3-D analysis is required to fully characterize (simulate) a device. However, 3-D simulation involves enormous computer power in addition to presenting a greater challenge in getting the algorithms to be stable or getting the solution iterations to converge since they are nonlinear [38]. As a result, 2-D analysis in which the discretisation involves dividing the device into grids is usually used [38, 39, 40]. 2-D simulation is more computer-friendly since it does not require as much computer power (processing power and memory requirement) as 3-D simulation [38]. To solve the device equations in 2-D, they must be discretised on the simulation grid. Thus the continuous functions of the partial differential equations, (PDEs), which make up the device equations, are represented by vectors of function values at the grid nodes, and the differential operators are replaced by suitable difference operators [38]. The simulation program can be efficient with regards to computer resources if the gridding is done in such a way that there are many grid points at places where there are steep gradients, and fewer grid points where the device does not change much [38, 39].

The primary function of device simulation programs such as Medici<sup>TM</sup>, is to solve the three basic set of partial differential equations (PDEs) which describe the device operation (device equations) for the electrostatic potential ( $\psi$ ) and for the electron and hole concentrations,  $n$  and  $p$  respectively [39]. The three sets of device equations are [16], [18], [38-52]:

1. The Poisson's equation, which relates the local charge (i.e. space charge) to the local electrostatic potential, governs the electrical behavior of semiconductor devices.
2. The current density equations, which describe the carrier fluxes.
3. The continuity equations, which preserves continuity by ensuring that the balance of generation and recombination with current changes between grid elements (or volume elements for 3-D device) is preserved.

#### 1. Poisson's equation

Poisson's is given by

$$\nabla^2 \psi = -\frac{q}{\epsilon_s} (p - n + N_D^+ - N_A^-) - \frac{\rho_s}{\epsilon_s} \quad (4.1)$$

where:  $\psi$  = local potential =  $\frac{E_F - E_{Fi}}{q}$

$n$  = electron concentration

$p$  = hole concentration

$N_D^+$  = concentration of ionized donor impurities

$N_A^-$  = concentration of ionized acceptor impurities

$\rho_s$  = surface charge density that may be present on the surface of device

$\epsilon_s$  = permittivity of the semiconductor material

$q$  = electronic charge

$$\nabla^2 = \frac{\partial^2}{\partial x^2}$$

$E_F$  = Electron or hole quasi-Fermi level

$E_{Fi}$  = Intrinsic Fermi level

Here, it should be noted that at the contacts to the device  $\psi$  is set equal to the applied voltage.

## 2. Current density equations

The set of current density equations is given by

$$\begin{aligned} J_n &= q\mu_n nE + qD_n \nabla n \\ J_p &= q\mu_p pE - qD_p \nabla p \end{aligned} \quad (4.2)$$

Equation (4.2) can be written alternatively in terms of  $\psi$  as

$$\begin{aligned} J_n &= -qn\mu_n \nabla \psi + qD_n \nabla n \\ J_p &= -qp\mu_p \nabla \psi - qD_p \nabla p \end{aligned} \quad (4.3)$$

where:  $E = -\nabla\psi = -\frac{\partial\psi}{\partial x}$  = electric field = potential gradient.

$J_n, J_p$  = electron and hole current densities respectively.

$\mu_n, \mu_p$  = mobilities of electrons and holes respectively.

$D_n, D_p$  = diffusion coefficients of electrons and holes respectively.

$$\nabla n = \text{electron concentration gradient} = \frac{\partial n}{\partial x}$$

$$\nabla p = \text{hole concentration gradient} = \frac{\partial p}{\partial x}$$

The current density equations give the fluxes of the charge carriers (electrons and holes).

They consist of a drift component caused by the electric field and a diffusion component caused by the carrier concentration gradient.

## 3. Continuity equations

The third set of equations is the continuity equations for electron and holes, which are given respectively by

$$\begin{aligned}\frac{1}{q} \nabla \cdot J_n &= (G_n - U_n) + \frac{\partial n}{\partial t} \\ \frac{1}{q} \nabla \cdot J_p &= (G_p - U_p) + \frac{\partial p}{\partial t}\end{aligned}\tag{4.4}$$

where,  $G_n, G_p$  = electron and hole generation rate respectively

$U_n$  = electron recombination rate in p-type material

$U_p$  = hole recombination rate in n-type material

The remaining quantities have their usual meaning. The continuity equations state that the current that goes into a volume element (or grid element for 2-D simulation) minus the current that comes out of it, which is symbolized by the del ( $\nabla$ ) operator, equals the net generation rate plus the rate of charge build up in that volume (or area) [38]. The electron and hole generation rates ( $G_n$  and  $G_p$ ) are caused by external influences such as optical excitation with high-energy photons, impact ionization under large electric fields, and thermal excitation [39].

Simulation programs calculate a steady-state solution when all device equations are satisfied for all the volume elements (for 3-D) and grid elements (for 2-D) in the device structure. This means that, currents must match both the electric fields and carrier concentration gradients that exist between neighboring elements [38, 39, 40]. Since the continuity equations allow for time evolution as given by the time derivatives of the carrier concentrations, the system of device equations has to be discretised over time and

transient solutions performed. The resulting equations are a set of algebraic equations, which are coupled and nonlinear. As a result, the equations cannot be solved directly in one step, but starting from an initial guess, they are solved by a nonlinear iteration method [38, 39, 40].

An initial guess is first calculated by assuming no current divergence, which gives an initial concentration and potential distribution. A repetitive update of electron and hole concentrations and potential then follows through an iteration of solutions of the carrier flux and continuity equations. In the simulation process, contacts to the device and their associated voltages have to be provided and these are specified in the input file in addition to any special conditions that may prevail at the contacts and device boundaries. If the voltages at the contacts are zero, the simulation program converges to a solution rather quickly and a Poisson solution alone is sufficient [38, 39]. For extreme biasing conditions, the program takes a longer time to converge to a steady-state solution and there is the added danger that no convergence is reached [38, 39]. For the I-V characteristics of field effect transistors (FETs), only one carrier (electrons or holes) is considered in the solution since FETs are majority carrier devices and minority carrier currents are negligible [38, 39, 42, 43, 44]. However, both carriers (electrons and holes) have to be considered in the simulation of bipolar junction devices (BJTs and p-n junction diodes) and breakdown simulations of FETs [39]. In general non-equilibrium and non-steady state solutions are needed.

## 4.2 Device Simulation with Traps

If carrier recombination and generation via trap centers are considered in devices containing traps then the device equations have to be modified to account for the trapping and de-trapping processes that take place in the semiconductor material. Both shallow level and deep level traps may be simulated, and there are basically four trap possibilities that can be simulated. These are neutral electron traps, neutral hole traps, donor traps, and acceptor traps [38]. The ionized charge state of the traps are very important, since the charged state of the traps has to be included in the trap statistics before they are incorporated in the device equations, particularly Poisson's and the continuity equations [16,18, 39, 42-52].

In the case of electron traps, if the trap levels are below the electron Fermi level, then the traps are filled with bound electrons and the ionized charge state is negative. Trap levels above the electron Fermi level will be empty of electrons, and the charge state of the traps will be neutral. For hole traps, if the trap levels are above the hole Fermi level, then the traps will be filled with bound holes and their ionized charge state is positive since holes are attributed with positive charge. Hole traps below the hole Fermi level will be devoid of holes (empty of holes but contain electrons) and they therefore have a neutral charge state since the negative charge of electrons will cancel out the positive charge of the holes. Here, electron and hole Fermi levels refer to electron and hole quasi Fermi levels.

Donor traps with energy levels above the electron Fermi level will be devoid of electrons and as a result have a positive charge state, just like donor impurities that have

contributed their valence electrons to the conduction band. If the energy levels of donor traps are, however, below the electron Fermi level, then the traps will be filled with electrons and the net charge state of the traps is zero (neutral charge state) just as in the case of donor impurities. In the case of acceptor traps, if the trap levels are above the hole Fermi level, they are filled with holes and their charge state is neutral as in acceptor impurities. If the energy levels of the acceptor traps are below the hole Fermi level, then they are empty of holes (filled with electrons), and therefore their ionized charge state is negative, as in the case of acceptor impurities.

Thus a donor trap can either capture an electron (emit a hole) and have a neutral charge state, or emit an electron (capture a hole) and be in a positive ionized charge state [16, 18, 39, 42-52]. An acceptor trap can either capture an electron (emit a hole) and possess a negative charge or emit electron (capture a hole) and be in the neutral charge state (have zero net charge) [16, 18, 39, 42-52]. In device simulation, donor traps and/or acceptor traps are considered and incorporated in the device equations.

Trapping of carriers and carrier recombination and generation through deep level traps are modeled by the Shockley-Read-Hall (SRH) statistics, and are described by four transition processes [40] which are: electron capture ( $K_n$ ), electron emission ( $E_n$ ), hole capture ( $K_p$ ), and hole emission ( $E_p$ ). The transition processes can be written as,

$$K_n = \frac{1}{\tau_{cn}} n(1 - f_T) \quad (4.5)$$

$$E_n = \frac{1}{\tau_{en}} N_T f_T \quad (4.6)$$

$$R_n = K_n - E_n \quad (4.7)$$

$$K_p = \frac{1}{\tau_{cp}} pf_T \quad (4.8)$$

$$E_p = \frac{1}{\tau_{ep}} N_T (1 - f_T) \quad (4.9)$$

$$R_p = K_p - E_p \quad (4.10)$$

Where  $N_T$  is the trap density (number/cm<sup>3</sup>) for a particular trap level,  $f_T$  is probability of trap occupancy for the trap level with a maximum value of unity.  $R_n$  and  $R_p$  are the net electron and hole recombination rates, respectively. Under steady-state conditions, the electron and hole recombination rates ( $R_n$  and  $R_p$ ) are equal and are given by [18],

$$R_n = R_p = \frac{np - n_{ie}^2}{\tau_{cp}(n + n_1) + \tau_{cn}(p + p_1)} \quad (4.11)$$

The trap occupation probability is then given by [18], [50],

$$f_T = \frac{\tau_{cp}n + \tau_{cn}p_1}{\tau_{cp}(n + n_1) + \tau_{cn}(p + p_1)} \quad (4.12)$$

Here,  $n_1$  and  $p_1$  are the electron and hole concentrations when the Fermi level ( $E_F$ ) and the trap energy level ( $E_T$ ) coincide in which case

$$n_1 = n_{ie} \exp\left(\frac{E_T - E_i}{kT}\right) \quad (4.13)$$

$$p_1 = \frac{n_i^2}{n_1} = n_{ie} \exp\left(\frac{E_i - E_T}{kT}\right) \quad (4.14)$$

where  $E_i$  and  $n_{ie}$  are the intrinsic Fermi level and intrinsic carrier concentration respectively,  $k$  is the Boltzman's constant and  $T$  is the absolute temperature.

When deep level traps are present in a semiconductor device, the basic equations used to determine the device characteristics for the two-carrier model are: 1) Poisson's equation, 2) continuity equations for electrons and holes, 3) current density equations for electrons and holes, and 4) rate equations for the deep levels [45].

1. Poisson's equation

(a) With deep donor traps present:

$$\nabla^2\psi = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^- + N_{Tdd}(1 - f_T)) - \rho_s \quad (4.15)$$

or,

$$\nabla^2\psi = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^- + N_{Tdd}^+) - \rho_s \quad (4.16)$$

Here  $N_{Tdd}$  and  $N_{Tdd}^+$  are the neutral deep donor and ionized deep donor trap concentrations respectively, and  $N_{Tdd}^+ = N_{Tdd}(1 - f_T)$ .  $\rho_s$  is the surface charge density that may be present on the surface of device.

(b) With deep acceptor traps present:

$$\nabla^2\psi = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^- - N_{Tda}f_T) - \rho_s \quad (4.17)$$

or

$$\nabla^2\psi = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^- - N_{Tda}^-) - \rho_s \quad (4.18)$$

Where  $N_{Tda}$  and  $N_{Tda}^-$  are the neutral and ionized deep acceptor concentrations respectively, and  $N_{Tda}^- = N_{Tda}f_T$ .

(c) With both deep donors and acceptors present:

In a device where both deep donors and deep acceptors are present, Poisson's equation becomes:

$$\nabla^2 \psi = -\frac{q}{\epsilon} (p - n + N_D^+ - N_A^- + N_{Tdd}(1 - f_T) - N_{Tda} f_T) - \rho_s \quad (4.19)$$

or

$$\nabla^2 \psi = -\frac{q}{\epsilon} (p - n + N_D^+ - N_A^- + N_{Tdd}^+ - N_{Tda}^-) - \rho_s \quad (4.20)$$

## 2. Continuity equations for electrons and holes

(a) With deep donor traps present: Electrons

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - \left[ \frac{1}{\tau_{cn}} N_{Tdd} (1 - f_T) n - \frac{1}{\tau_{en}} N_{Tdd} f_T \right] \quad (4.21)$$

or

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - [C_n N_{Tdd}^+ n - e_n (N_{Tdd} - N_{Tdd}^+)] \quad (4.22)$$

(b) With deep donor traps present: Holes

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - \left[ \frac{1}{\tau_{cp}} N_{Tdd} f_T p - \frac{1}{\tau_{ep}} N_{Tdd} (1 - f_T) \right] \quad (4.23)$$

or

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - [C_p (N_{Tdd} - N_{Tdd}^+) p - e_p N_{Tdd}^+] \quad (4.24)$$

(c) With deep acceptors present: Electrons

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - \left[ \frac{1}{\tau_{cn}} N_{Tda} (1 - f_T) n - \frac{1}{\tau_{en}} N_{Tda} f_T \right] \quad (4.25)$$

or

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - [C_n (N_{Tda} - N_{Tda}^-) n - e_n N_{Tda}^-] \quad (4.26)$$

(d) With deep acceptors present: Holes

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - \left[ \frac{1}{\tau_{cp}} N_{Tda} f_T p - \frac{1}{\tau_{ep}} N_{Tda} (1 - f_T) \right] \quad (4.27)$$

or

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - [C_p N_{Tda}^- p - e_p (N_{Tda} - N_{Tda}^-)] \quad (4.28)$$

(e) With both deep donors and acceptors present: Electrons

$$\begin{aligned} \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - \left\{ \frac{1}{\tau_{cn}} N_{Tdd} (1 - f_T) n + \frac{1}{\tau_{cn}} N_{Tda} (1 - f_T) n \right. \\ \left. - \frac{1}{\tau_{en}} N_{Tdd} f_T - \frac{1}{\tau_{en}} N_{Tda} f_T \right\} \end{aligned} \quad (4.29)$$

or

$$\begin{aligned} \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - [C_n N_{Tdd}^+ n + C_n (N_{Tda} - N_{Tda}^-) n \\ - e_n (N_{Tdd} - N_{Tdd}^+) - e_n N_{Tda}^-] \end{aligned} \quad (4.30)$$

(f) With both deep donors and acceptors present: Holes

$$\begin{aligned} \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - \left[ \frac{1}{\tau_{cp}} N_{Tdd} f_T p + \frac{1}{\tau_{cp}} N_{Tda} f_T p \right. \\ \left. - \frac{1}{\tau_{ep}} N_{Tdd} (1 - f_T) - \frac{1}{\tau_{ep}} N_{Tda} (1 - f_T) \right] \end{aligned} \quad (4.31)$$

or

$$\begin{aligned} \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - [C_p (N_{Tdd} - N_{Tdd}^+) p + C_p N_{Tda}^- p \\ - e_p N_{Tdd}^+ - e_p (N_{Tda} - N_{Tda}^-)] \end{aligned} \quad (4.32)$$

In the above equations,  $C_n$  and  $C_p$  are electron and hole capture coefficients respectively and  $e_n$  and  $e_p$  are electron and hole emission rates respectively of the deep level traps. These quantities are given by:

$$C_n = \sigma_n v_{nth} \quad C_p = \sigma_p v_{pth}$$

$$e_n = C_n N_C g^{-1} \exp\{(E_T - E_C)/kT\}$$

$$e_p = C_p N_V g \exp\{(E_V - E_T)/kT\}$$

$N_C$  and  $N_V$  are the conduction band and valence band densities of state respectively, and  $g$  is the degeneracy factor.  $\sigma_n$  and  $\sigma_p$  are the electron and hole capture cross-sections of the deep level trap centers respectively and  $v_{nth}$  and  $v_{pth}$  are the electron and hole thermal velocities respectively.

### 3. Current equations for electrons and holes

$$J_n = -q\mu_n n \nabla \psi + qD_n \nabla n \quad (4.33)$$

$$J_p = -q\mu_p p \nabla \psi - qD_p \nabla p \quad (4.34)$$

In transient analysis the traps should be modeled as time dependent since it takes time for the traps to capture and emit carriers (electrons and holes) and the traps require some time to come into equilibrium with the semiconductor material [39]. For the time dependent case the electron and hole net recombination rates ( $R_n$  and  $R_p$ ) are different and an additional partial differential equation (the rate equation for traps) relating the trap occupation and recombination rates must be solved [18, 39, 42, 44, 48, 51].

#### 4. Rate equation for the deep level traps

For the case of electron traps (and acceptors) the rate equation is given by [18, 39, 42, 44, 48, 51]:

(a) With deep donor traps present:

$$\begin{aligned} \frac{\partial(N_{Tdd} f_T)}{\partial t} &= R_n(t) - R_p(t) \\ \frac{\partial(N_{Tdd} f_T)}{\partial t} &= \left[ \frac{1}{\tau_{cn}} N_{Tdd} (1 - f_T) n - \frac{1}{\tau_{en}} N_{Tdd} f_T \right] \\ &- \left[ \frac{1}{\tau_{cp}} N_{Tdd} f_T p - \frac{1}{\tau_{ep}} N_{Tdd} (1 - f_T) \right] \end{aligned} \quad (4.35)$$

or

$$\begin{aligned} \frac{\partial(N_{Tdd} - N_{Tdd}^+)}{\partial t} &= [C_n N_{Tdd}^+ n - e_n (N_{Tdd} - N_{Tdd}^+)] \\ &- [C_p (N_{Tdd} - N_{Tdd}^+) p - e_p N_{Tdd}^+] \end{aligned} \quad (4.36)$$

(b) With deep acceptor traps present:

$$\begin{aligned} \frac{\partial(N_{Tda} f_T)}{\partial t} &= R_n(t) - R_p(t) \\ \frac{\partial(N_{Tda} f_T)}{\partial t} &= \left[ \frac{1}{\tau_{cn}} N_{Tda} (1 - f_T) n - \frac{1}{\tau_{en}} N_{Tda} f_T \right] \\ &- \left[ \frac{1}{\tau_{cp}} N_{Tda} f_T p - \frac{1}{\tau_{ep}} N_{Tda} (1 - f_T) \right] \end{aligned} \quad (4.37)$$

or

$$\begin{aligned} \frac{\partial(N_{Tda}^-)}{\partial t} &= [C_n (N_{Tda} - N_{Tda}^-) n - e_n N_{Tda}^-] \\ &- [C_p N_{Tda}^- p - e_p (N_{Tda} - N_{Tda}^-)] \end{aligned} \quad (4.38)$$

The above trapping and generation-recombination models are incorporated into the semiconductor device equations in order to simulate and investigate trapping phenomena in semiconductor devices.

#### 4.3 Procedure and Results of MESFET Device Simulation

Device simulation using the two-dimensional device simulator Medici™ was used to help explain the discrepancy between the experimental DC drain I-V characteristics measurements and the results of TAS, thermal DLTS and thermal output conductance measurements. The basic device structure of the MESFET without p-buffer layer simulated in this study is shown in Figure 4.1.

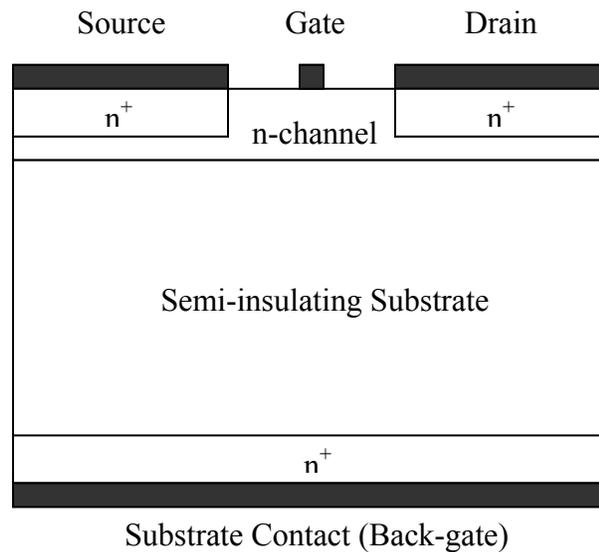


Figure 4.1: Device structure of SiC MESFET on semi-insulating (SI) substrate without a p-buffer layer used in the simulation.

In Figure 4.2 the basic device structure of the MESFET with p-buffer layer simulated in this study is depicted. The vanadium doped SI substrate is modeled by

doping the substrate n-type with a concentration of  $1 \times 10^{15} \text{ cm}^{-3}$  and compensating it with  $5 \times 10^{16} \text{ cm}^{-3}$  deep level acceptor traps at energy level 0.63 eV above midgap [5, 6, 7, 12]. This results in the SI substrate having a resistivity on the order of  $1 \times 10^{12} \Omega\text{-cm}$ . The acceptor trap energy level of 0.63 eV above mid-gap was selected because this was approximately what was measured for the vanadium acceptor level in the TAS, DLTS, and output conductance measurements in the experimental characterization [35]. Moreover as reported in the literature, vanadium has two levels in 4H-SiC: an acceptor level at about an energy level that ranges from  $E_C - 0.8 \text{ eV}$  to  $E_C - 1.1 \text{ eV}$ , about 0.50 – 0.8 eV above mid-gap using 4H-SiC band gap of 3.2 eV, and a donor level at roughly mid-gap [53, 54, 55, 56, 57, 58, 60].

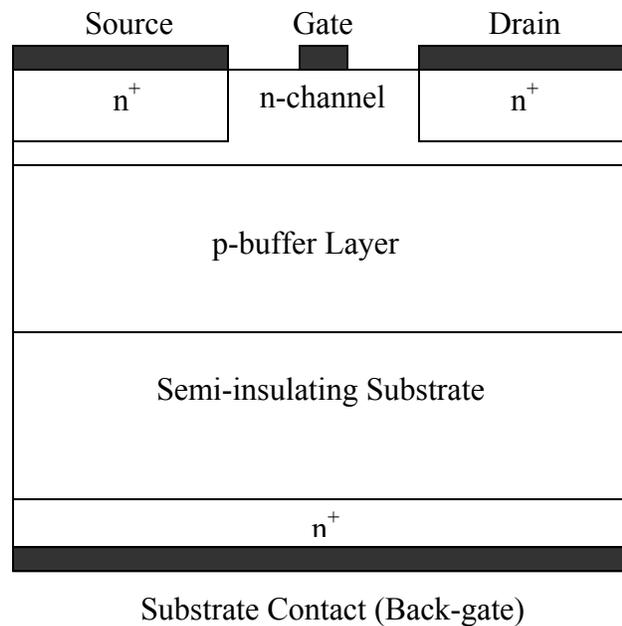


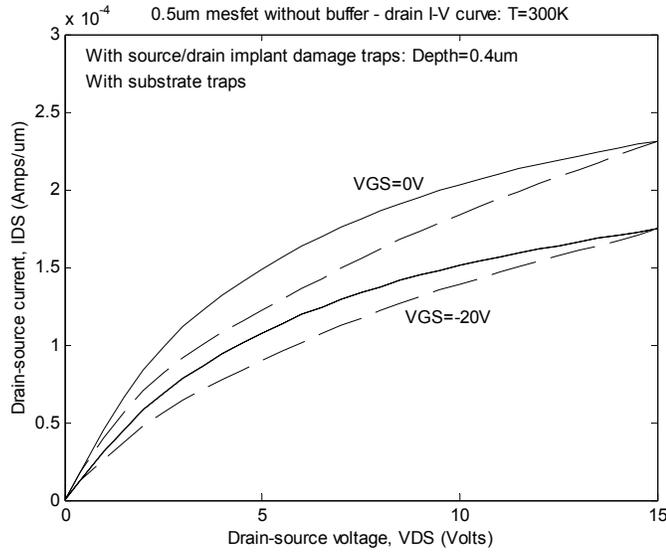
Figure 4.2: Device structure of SiC MESFET on semi-insulating (SI) substrate with p-buffer layer used in the simulation.

Since the source and drain contact regions were implanted, there will be lattice damage due to the implantation. The implant damage results in deep level acceptor-like traps with energy levels distributed throughout the (upper half) SiC band gap [8, 9, 10, 11, 24]. To model the source/drain implant damage, acceptor traps with distributed energy levels in the band gap were used. The spatial distribution of the implant damage traps has a depth of 0.4  $\mu\text{m}$  from the surface, covers the source and drain regions, and stretches out 0.5  $\mu\text{m}$  from the inside edges of the source and drain into the un-gated channel region. The 0.5  $\mu\text{m}$  extension accounts for lateral straggle (standard deviation) of the implant species, which occurs under the implant mask [59]. The estimated depth of source/drain implant is 0.2  $\mu\text{m}$ , however, the depth of traps used to model the implant damage was 0.4  $\mu\text{m}$ . This is because, as pointed out by Koshka et al. [13], implant damage can extend beyond the projected range of the implanted species by about as much as twice the projected range. Furthermore, most implant damage occurs at the edges of the implanted area [59].

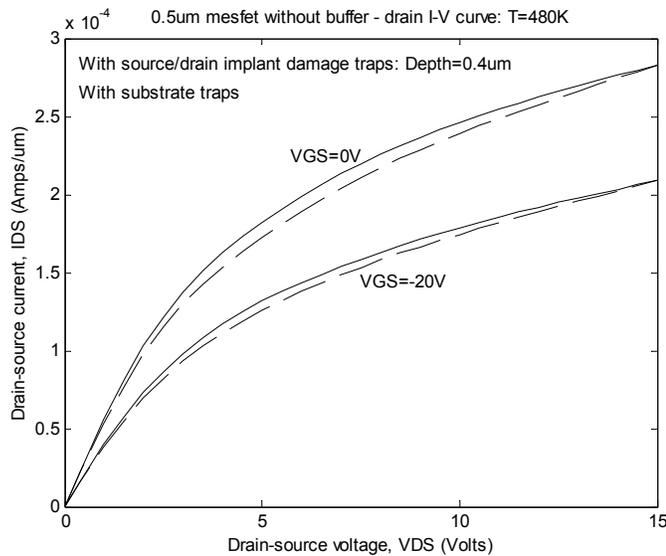
In this simulation, the source and substrate voltages were kept at 0 V. For the drain voltage, a transient triangular pulse with 15 V amplitude and 15.012480 s pulse width was used. The gate voltages ranged from 0 V to -20 V in steps of -5 V. The 15 V amplitude was the maximum drain voltage used in the experimental device drain I-V characteristics and 15.012480 s pulse width is the estimated time used in the experimental measurement for the drain voltage to go from 0V to 15 V and back to 0 V. For brevity, only the  $V_{GS}=0$  V and  $V_{GS}=-20$  V curves will be shown.

#### **4.3.1 Simulation of MESFET without P-buffer Layer with Traps Representing Source/Drain Implant Damage Traps and SI Substrate Traps**

Figure 4.3 shows the drain I-V curves obtained from transient simulation of the device without p-buffer at 300 K and 480 K with both substrate traps and source/drain implant damage traps. It can be seen that hysteresis decreases at 480 K as electrons are thermally emitted from trap centers. It should also be observed that the hysteresis decreases as  $V_{GS}$  becomes more negative due to the repulsion of electrons from the channel region with decreasing  $V_{GS}$ .



(a)

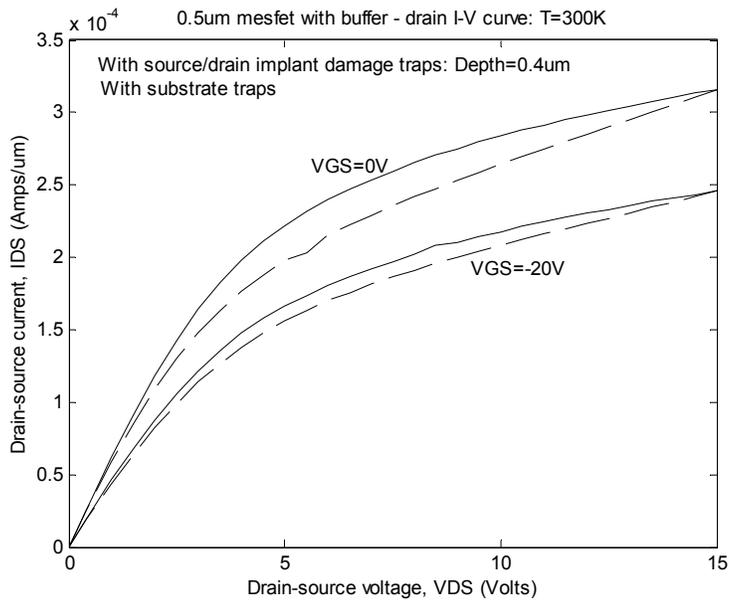


(b)

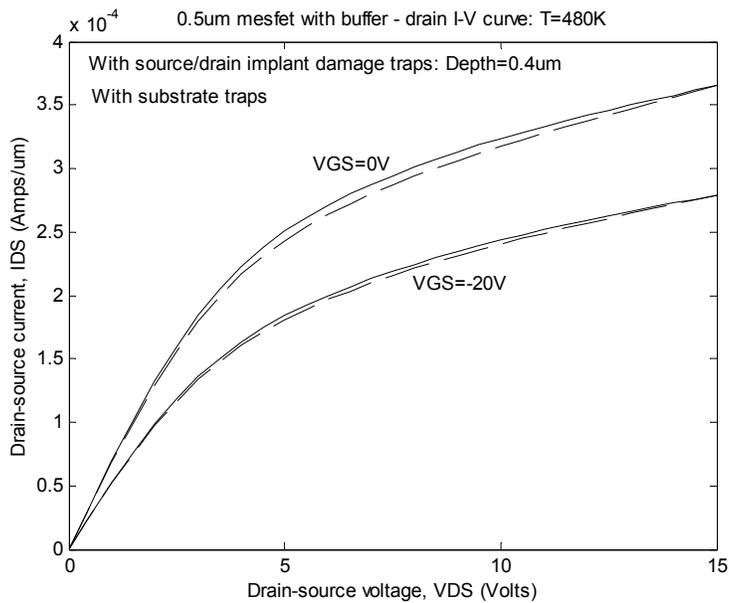
Figure 4.3: Simulated drain I-V characteristics of MESFET without p-buffer with traps representing source/drain implant damage and semi-insulating substrate traps at (a) 300 K and (b) 480 K.

#### **4.3.2 Simulation of MESFET with P-buffer Layer with Traps Representing Source/Drain Implant Damage Traps and SI Substrate Taps**

The simulated drain I-V characteristics of the device with p-buffer layer with both substrate traps and source/drain residual implant damage traps at 300 K and 480 K are shown in Figure 4.4 (a) and (b) respectively. It can be observed that the degree of hysteresis in the device with p-buffer layer is about the same as in the device without the buffer at 300 K and 480 K respectively as observed in the experimental characterization, although they appear slightly reduced in the former. Furthermore, current levels are higher in the device with p-buffer than in the device without the buffer. Since the only difference between the two devices is the presence of the p-buffer layer in one of them, this suggests that the p-buffer layer provides some degree of isolation of the channel electrons from the semi-insulating substrate traps. In addition, the hysteresis decreases with increasing negative  $V_{GS}$  as in the simulated I-V curves of the device without buffer.



(a)



(b)

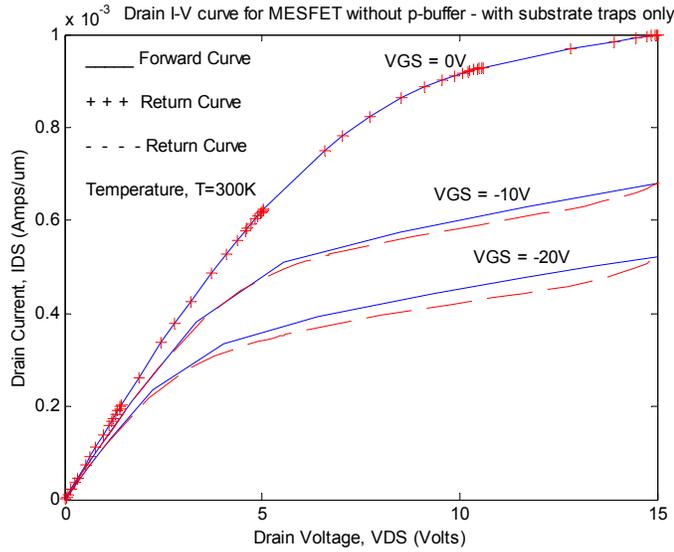
Figure 4.4: Simulated drain I-V characteristics of MESFET with p-buffer, with traps representing source/drain residual implant lattice damage traps and SI substrate traps at (a) 300 K and (b) 480 K.

### 4.3.3 Simulation of MESFETs with SI Substrate Traps only

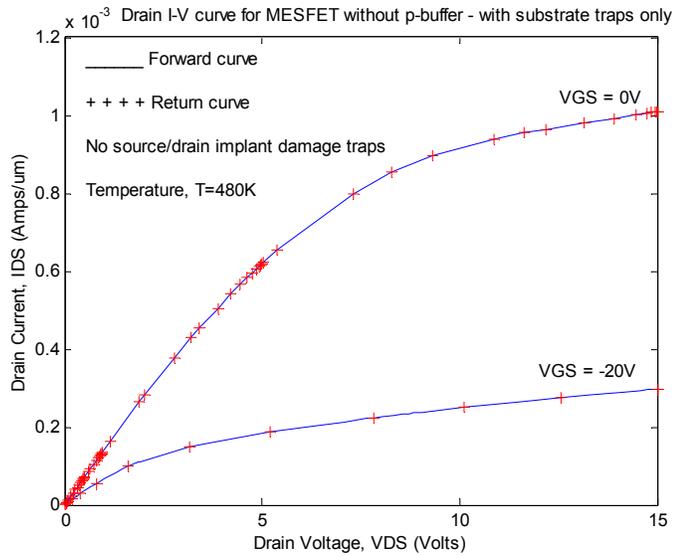
In order to determine the relative contributions of implant damage traps and SI substrate traps to the overall hysteresis, the simulation was performed with SI substrate traps only and no source/drain implant damage traps for both the device with p-buffer and the one without p-buffer, and then performed again with traps representing source/drain implant damage traps only and no SI substrate traps for a MESFET on p-type conductive substrate. For the study of the contribution of only source/drain residual implant damage traps, the simulation was performed on a MESFET with p-type conductive substrate to reduce substrate current since the device is n-channel. This helps to restrict the drain current mainly to the n-channel because of the potential barrier at the channel-substrate interface, due to the p-n junction of the substrate-channel interface, and also allows for greater gate control of the drain current.

Figure 4.5 shows the simulated drain I-V characteristics of a MESFET device without p-buffer layer with only substrate traps (no traps representing source/drain residual implant lattice damage) at 300 K and 480 K, and Figure 4.6 depicts the simulated drain I-V characteristics of a MESFET device with p-buffer layer with only SI substrate traps at 300 K and 480 K. At 300 K the hysteresis in the drain I-V curves of the device without p-buffer is more pronounced than for the device with p-buffer especially at high negative gate voltages, indicating the effectiveness of the p-buffer layer in isolating the channel electrons from the SI substrate traps, as already observed in the experimental measurements and also observed in the OAS measurement results covered in Chapter V. The hysteresis increases as the gate voltage increases negatively in both types of devices

since channel electrons are increasingly repelled deeper into the substrate as the gate voltage decreases.

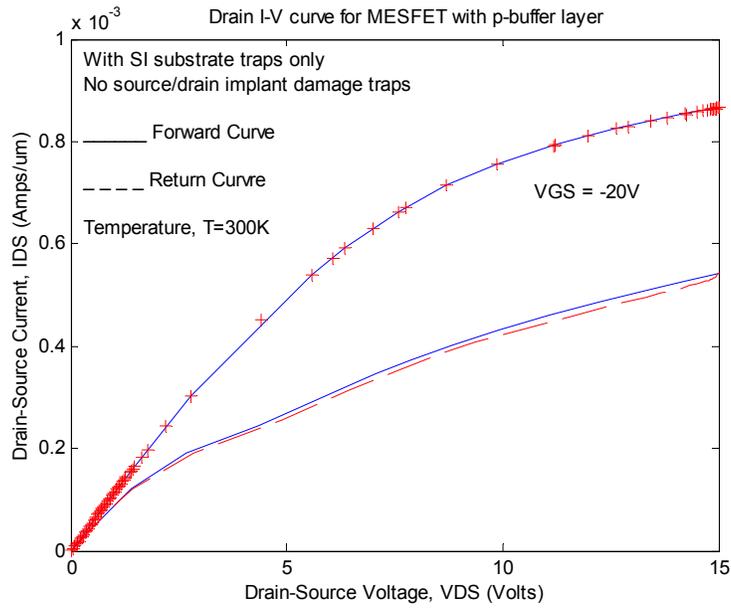


(a)

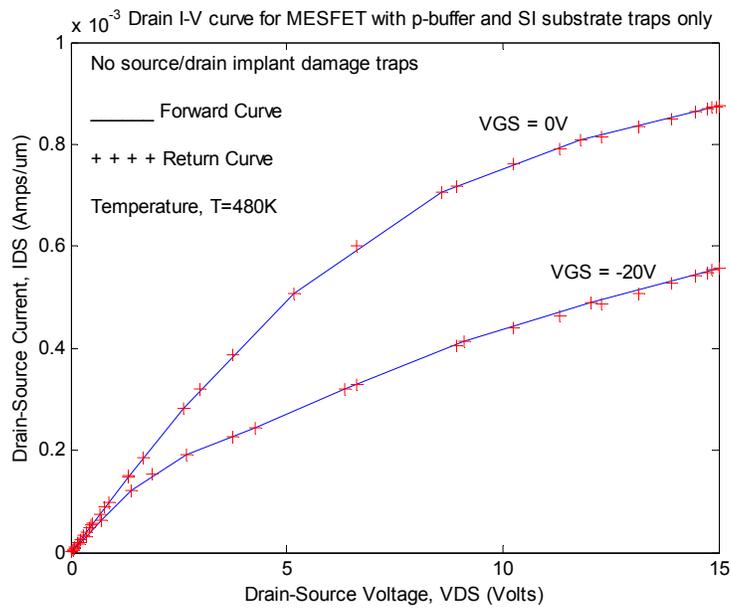


(b)

Figure 4.5: Simulated drain I-V characteristics of MESFET without p-buffer layer with only SI substrate traps at (a) 300 K (b) 480 K. No source/drain residual implant damage traps.



(a)



(b)

Figure 4.6: Simulated drain I-V characteristics of a MESFET with p-buffer layer with only SI substrate traps at (a) 300 K and (b) 480 K.

At 480 K, hysteresis disappears completely in the I-V curve of both types of devices, suggesting that the hysteresis at 480 K is not due to SI substrate traps but mainly due to trapping related to source/drain residual implant lattice damage. Thus, it is quite plausible that the hysteresis that remains at 480 K in the experimental drain I-V characteristics is due to source/drain residual implant lattice damage traps.

#### **4.3.4 Simulation of MESFET with Traps Representing Source/Drain Residual Implant Lattice Damage Traps only**

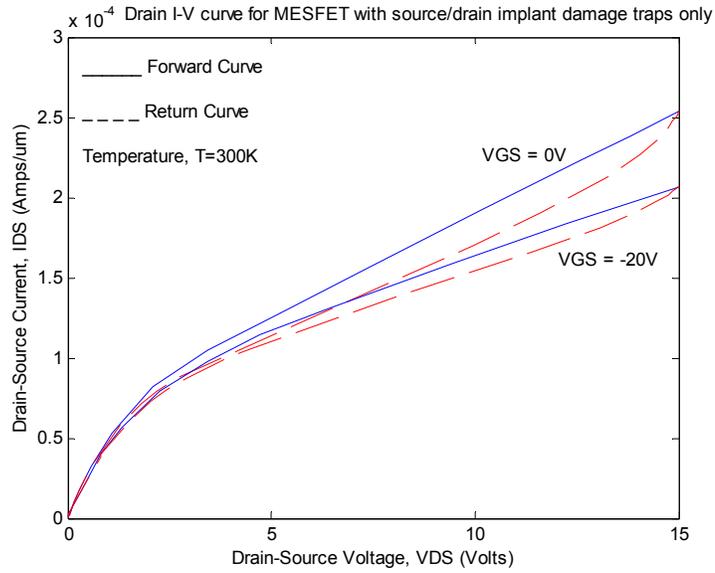
To investigate the effects of the source and drain residual implant damage traps on MESFET drain I-V characteristics, a simulation n-channel MESFET was built on p-type conductive substrate with shallow doping concentration of  $1 \times 10^{15} \text{ cm}^{-3}$  without any substrate traps. This restricts the drain current as much as possible to the channel area because of the interface potential barrier of the substrate-channel p-n junction, and enables the effects of the source/drain implant damage traps to be studied. The concentration of traps, representing residual implant damage traps, used in the simulation is  $8 \times 10^{16} \text{ cm}^{-3}$ . This implant damage trap concentration is selected because according to Mitra et al. [10], the concentration of traps  $N_t$  due to implant lattice damage could be as much as 1% of the net carrier volumetric concentration,  $N_s$ , as already mentioned in Chapter I, section 1.3. That is  $N_t = 0.01N_s$ . Hence with the net carrier concentration of the source and drain implanted ohmic contact regions of  $1 \times 10^{19} \text{ cm}^{-3}$ , a trap concentration of  $8 \times 10^{16} \text{ cm}^{-3}$  is a reasonable choice, noting that 1% of  $1 \times 10^{19} \text{ cm}^{-3}$  is  $1 \times 10^{17} \text{ cm}^{-3}$ . The traps have distributed energy levels in the SiC band gap and the trap spatial distribution extends from  $x = 0 \text{ }\mu\text{m}$  to  $x = 16.5 \text{ }\mu\text{m}$  on the source side and  $x = 23.5 \text{ }\mu\text{m}$  to  $x = 40 \text{ }\mu\text{m}$

on the drain side. The depth of the trap distribution at both the source and drain sides is  $0.4 \mu\text{m}$  from the device surface (i.e.,  $y = 0.4 \mu\text{m}$ ). Here, it should be noted that the dimensions of the source and drain regions are  $x = 16 \mu\text{m}$  by  $y = 0.2 \mu\text{m}$ , which are the dimensions of the source and drain ohmic contact regions of the experimental MESFETs. The  $0.4 \mu\text{m}$  trap depth distribution was selected because according to Koshka et al. [13] implant lattice damage can extend beyond the projected range by as much as two times the nominal value.

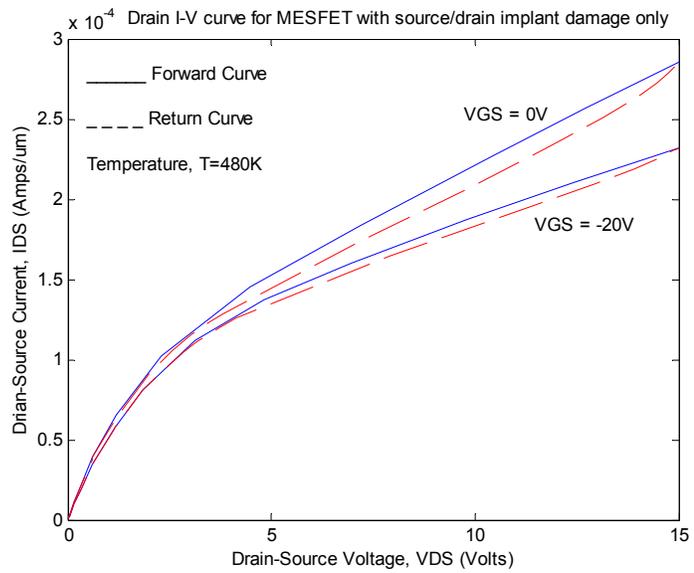
Figures 4.7(a) and (b) show the simulated drain I-V characteristics of MESFET on p-substrate with traps simulating only source/drain residual implant damage traps (no substrate traps) at 300 K and 480 K, respectively. At 480 K, hysteresis still persists in the drain I-V characteristics even though the hysteresis is reduced relative to that at 300 K. As in the case of the simulated devices with both SI substrate traps and source/drain implant damage traps, the hysteresis also decreases as  $V_{GS}$  decreases (increases negatively) in the simulated devices with only source/drain implant damage traps. The foregoing observation coupled with the observation that the hysteresis vanishes at 480 K in the simulated device with only substrate traps lead to the conclusion that, acceptor-type source/drain implant damage traps are major contributors to the hysteresis at 300 K and are solely responsible for the hysteresis at 480K in the drain I-V curves of the experimental devices.

Comparing Figure 4.3, Figure 4.4, and Figure 4.7 to Figures 3.1 and 3.2, the drain I-V curves for the experimental MESFETs at 300 K and 480 K respectively, it can be seen that the hysteresis in the experimental I-V curves at 480 K in Figure 3.2 decreases

with decreasing  $V_{GS}$ , just as in the simulated I-V curves for MESFETs with both SI substrate traps and source/drain implant damage traps and MESFETs with only source/drain implant damage traps at 300 K and 480 K. This reinforces the conclusion that the hysteresis at high temperatures (such as 480 K) in the experimental devices is due to source/drain residual implant lattice damage traps, since all the hysteresis in the simulated drain I-V curves of MESFETs with only SI substrate traps disappears at 480 K, as shown in Figures 4.5(b) and 4.6(b). From Figures 4.5(a) and 4.6(a), it can be seen that the hysteresis in the simulation drain I-V curves of MESFETs with only SI substrate traps increase with decreasing  $V_{GS}$  at 300 K. This suggests that some percentage of the hysteresis in the experimental drain I-V curves at very negative  $V_{GS}$  such as -20 V at 300 K in Figure 3.1 could be attributed to SI substrate traps, while much of the hysteresis at less negative  $V_{GS}$  could be attributed to source/drain implant damage traps. Furthermore, since hysteresis occurs to about the same degree in the experimental I-V curves of both the devices with buffer and those without buffer, then the SI substrate traps contribute comparatively little to the overall hysteresis and that much of the hysteresis is therefore due to source/drain residual implant damage traps, particularly at high temperatures such as 480 K.



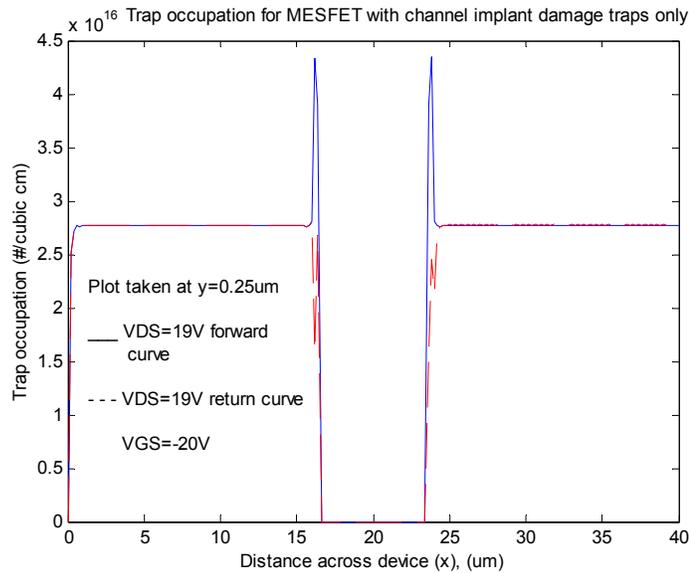
(a)



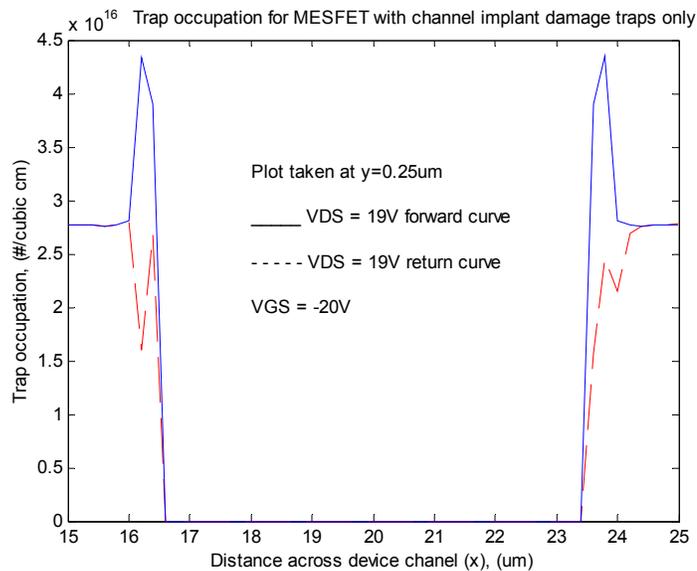
(b)

Figure 4.7: Simulated drain I-V characteristics of MESFET with traps representing only source/drain residual implant damage traps at (a) 300 K (b) 480 K.

For the MESFET with source/drain residual implant damage traps only, Figure 4.8 shows that the trapping and emission processes take place largely in the pencil of traps at the un-gated inside edges of the source and drain regions due to the lateral straggle (standard deviation) of implanted ions. In the simulation, these regions extend from 16.00  $\mu\text{m}$  to 16.50  $\mu\text{m}$  at the source side and 23.50  $\mu\text{m}$  to 24.00  $\mu\text{m}$  at the drain side. The lateral straggle is formed because of the statistical nature of the implantation process, leading to the implanted ions being scattered laterally and underneath the edges of the implant mask [59]. The lateral straggle is formed in addition to the vertical straggle, resulting in a 2-dimensional profile. Simulations show that the hysteresis in the drain I-V characteristics for MESFET with source/drain residual implant damage traps is due to the pencil of traps that results from the lateral straggle at the source and drain regions. No hysteresis occurs in the simulated drain I-V characteristics when the traps due to lateral straggle are reduced to zero, as will be shown later.



(a)



(b)

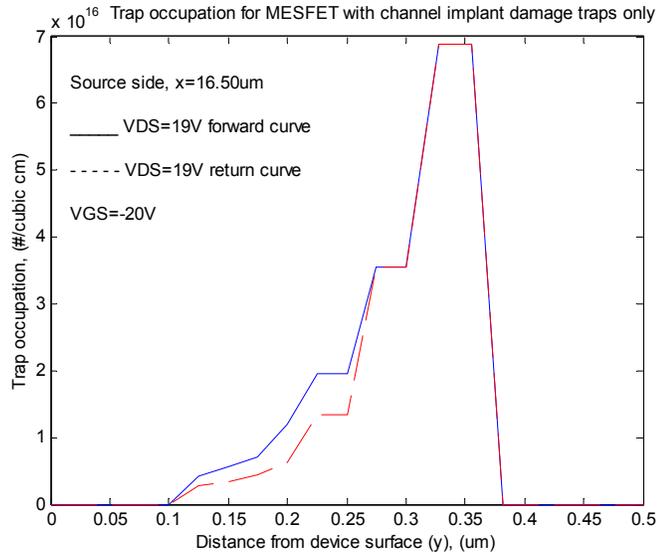
Figure 4.8: Trap occupation (empty, unoccupied trap centers) distribution across the channel for MESFET with only source/drain residual implant damage traps taken at a distance of 0.25  $\mu\text{m}$  from the device surface at 300 K for (a)  $0 \mu\text{m} < x < 40 \mu\text{m}$  (b)  $15 \mu\text{m} < x < 25 \mu\text{m}$ .

Figure 4.9 shows the 1-D trap occupation (empty, unoccupied trap centers) at distances of  $x = 16.25 \mu\text{m}$  and  $16.50 \mu\text{m}$  at the source side and Figure 4.10 shows the 1-D trap occupation (empty, unoccupied trap centers) at  $x = 23.50 \mu\text{m}$  and  $23.75 \mu\text{m}$  at the drain side. It is important to recognize in Figures 4.8, 4.9, and 4.10 that initially a box-like uniform distribution of empty traps is introduced at both the source and drain regions, simulating source/drain residual implant lattice damage traps. Hence the plots shown in Figures 4.8, 4.9, and 4.10 are actually the empty trap distributions remaining after electron capture. It is also crucial to note that electron emission is the dominant process as  $V_{\text{DS}}$  rises from 0 V to  $V_{\text{DS}(\text{max})}$  and electron capture is the dominant process as  $V_{\text{DS}}$  falls from  $V_{\text{DS}(\text{max})}$  to 0 V as discussed in Appendix A (Physics of Hysteresis). Thus as  $V_{\text{DS}}$  rises and falls there is an exchange of electrons between the occupied trap centers and empty trap centers. It is the difference in empty trap distributions as  $V_{\text{DS}}$  rises and falls at a given  $V_{\text{DS}}$  that leads to the hysteresis in the drain I-V curves. If there is no difference in the empty trap distributions as  $V_{\text{DS}}$  rises and falls there will be no hysteresis in the drain I-V curves.

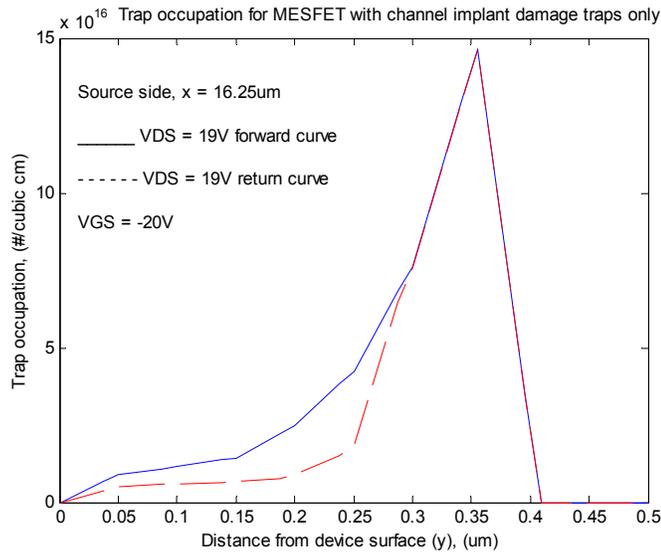
Both figures 4.9 and 4.10 show that the concentration of unoccupied (empty) trap centers on the return curve ( $V_{\text{DS}}$  falling from  $V_{\text{DS}(\text{max})}$  to 0 V) is less than that on the forward curve ( $V_{\text{DS}}$  rising from 0V to  $V_{\text{DS}(\text{max})}$ ) for a given  $V_{\text{DS}}$  at both the source and drain sides. This means that as  $V_{\text{DS}}$  falls, due to the capture dominant process, there are more electrons captured than on the forward curve (rising  $V_{\text{DS}}$ ) where electron emission dominates, as discussed in Appendix A (Physics of Hysteresis). On the other hand, as  $V_{\text{DS}}$  rises, due to the emission-dominant process, the concentration of electrons captured

is less leading to more unoccupied, empty, trap centers than on the return curve (falling  $V_{DS}$ ) where electron-capture dominates. This leads to higher free electron concentration on the forward curve as  $V_{DS}$  rises from 0 V to  $V_{DS(max)}$  and hence higher current levels than on the return curve as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V, resulting in a hysteresis in the drain I-V curve. Section 4.4 below discusses the physics of hysteresis as it applies to traps simulating source/drain residual implant lattice damage. A full discussion of the hysteresis due to both source/drain residual implant lattice damage and semi-insulating substrate traps is given in Appendix A.

Figures 4.11a and 4.11b show the 3-D empty trap distribution for MESFET with traps simulating only source/drain residual implant damage at  $V_{DS} = 19$  V for the forward and return curves respectively. A comparison of the figures indicates that the trapping and emission processes take place mainly in the pencil or volume of traps due to the lateral straggle of implanted ions, as already suggested. Figure 4.11b further shows that capture is the dominant process as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V, since the concentration of unoccupied trap centers is lower due to increased electron capture. There is no change in trap occupation outside the lateral straggle areas between the forward and return curves for a given  $V_{DS}$  as shown in Figures 4.8 and 4.11. Thus, although trapping mainly occurs at the channel side of the channel-substrate interface as shown in Figure 4.10, it is the trapping and emission processes that take place in the pencil or volume of traps due to the lateral straggle of implanted ions that lead to the hysteresis in the drain I-V characteristics for MESFET with traps representing source-drain residual implant damage traps only.

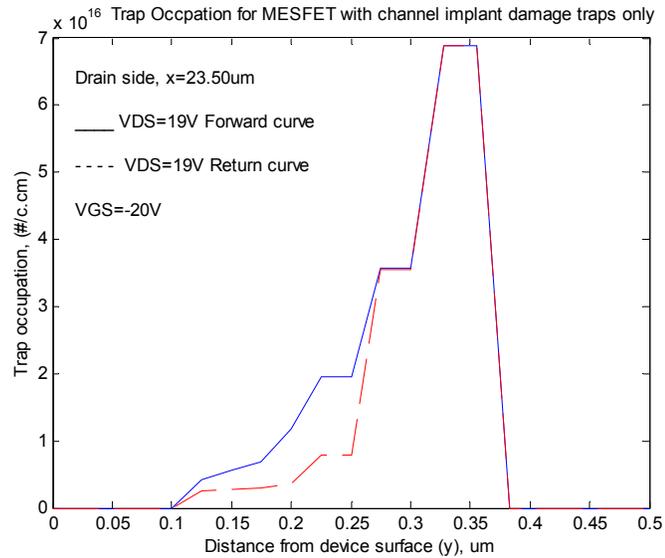


(a)

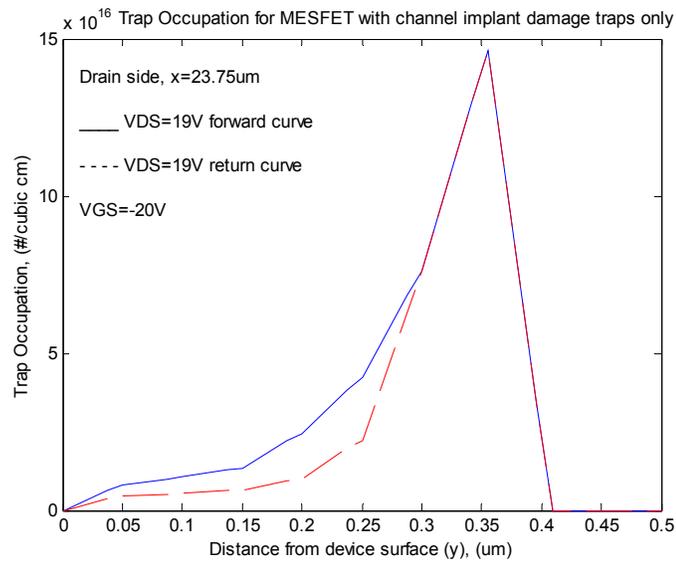


(b)

Figure 4.9: Trap occupation (empty, unoccupied trap centers) distribution for MESFET with only source/drain residual implant damage traps at the source side taken at (a)  $x = 16.5 \mu\text{m}$  and (b)  $x = 16.25 \mu\text{m}$ .

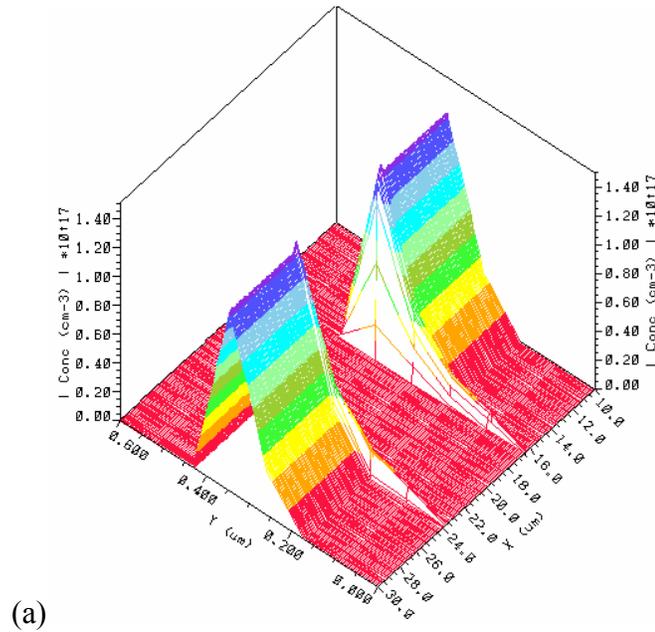


(a)

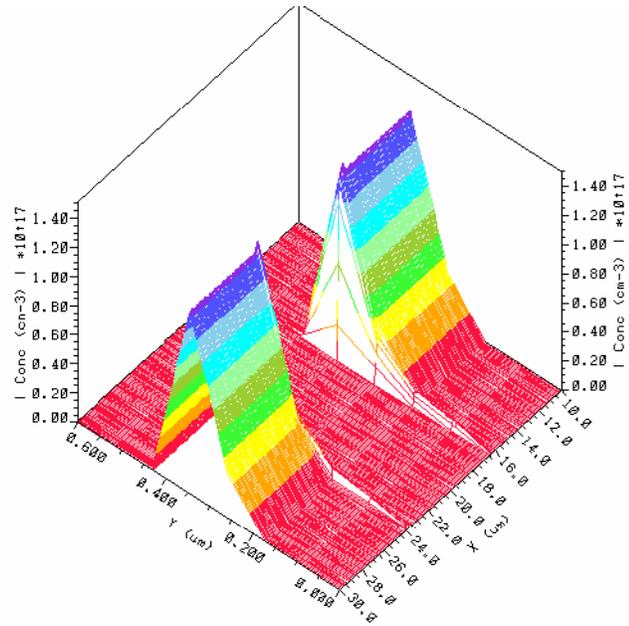


(b)

Figure 4.10: Trap occupation (empty, unoccupied trap centers) distribution for MESFET with only source/drain residual implant damage traps at the drain side taken (a)  $x = 16.5 \mu\text{m}$  and (b)  $x = 16.25 \mu\text{m}$ .



(a)



(b)

Figure 4.11: Trap occupation (empty, unoccupied trap centers) for MESFET with only source/drain residual implant damage traps for (a)  $V_{DS}=19$  V on the forward curve. Note the pencil of traps where most trapping and emission occur. (b)  $V_{DS}=19$  V on the return curve. Note the reduction in unoccupied trap concentration in the pencil of traps due to trapping.  $V_{GS} = -20$  V.

Figure 4.12 shows the drain I-V characteristics of a MESFET with source/drain residual implant lattice damage traps only but no traps due to lateral straggle implant damage. No hysteresis occurs in the simulated drain I-V characteristics. Figure 4.13 shows the 1-D trap occupation across the channel at  $0.25 \mu\text{m}$  below the device surface ( $y = 0.25 \mu\text{m}$ ) at  $V_{DS} = 19 \text{ V}$  on the forward and return curves, and  $V_{GS} = -20 \text{ V}$ . This is the same location as the trap occupation plot shown in Figure 4.8. As can be seen, the trap occupation is the same for both the forward and return curves, and there are no trapping and de-trapping processes taking place as the lateral straggle and its attendant traps have been reduced to zero.

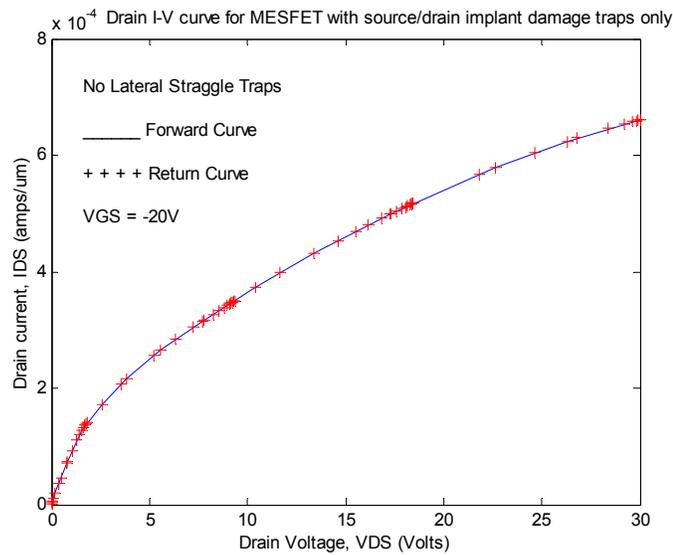


Figure 4.12: Drain I-V characteristics for MESFET with traps representing only source/drain residual implant damage, with traps due to lateral straggle of implanted ions reduced to zero. Note the absence of hysteresis in the I-V curve in contrast to Figure 4.7. Also note the increase in current compared to Figure 4.7 due to reduced trapping of channel electrons and reduction in channel resistance due to defect traps.

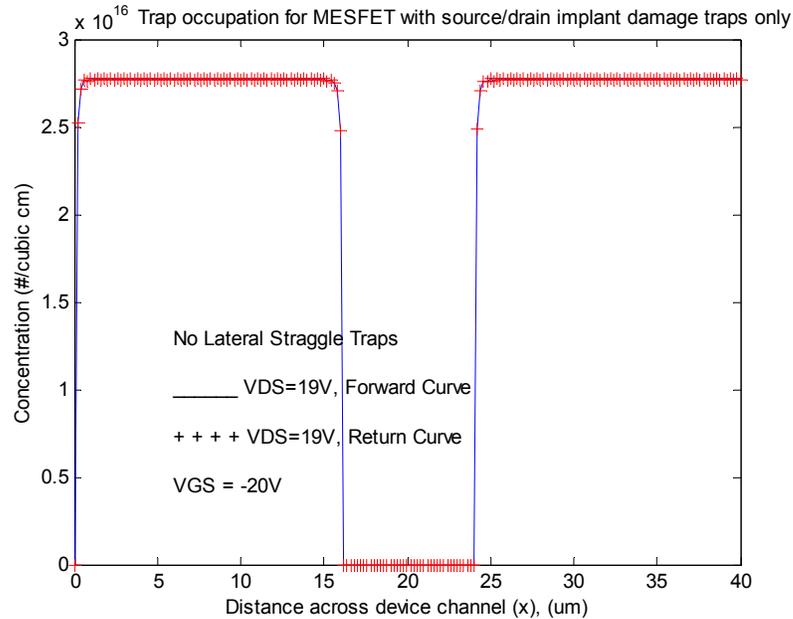
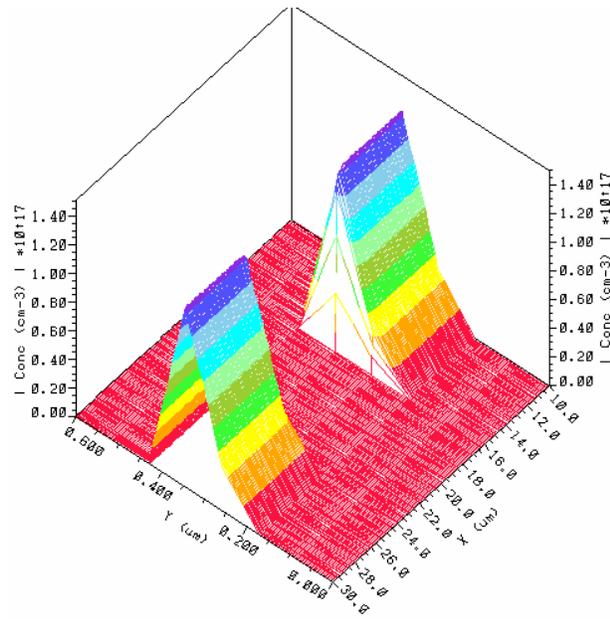
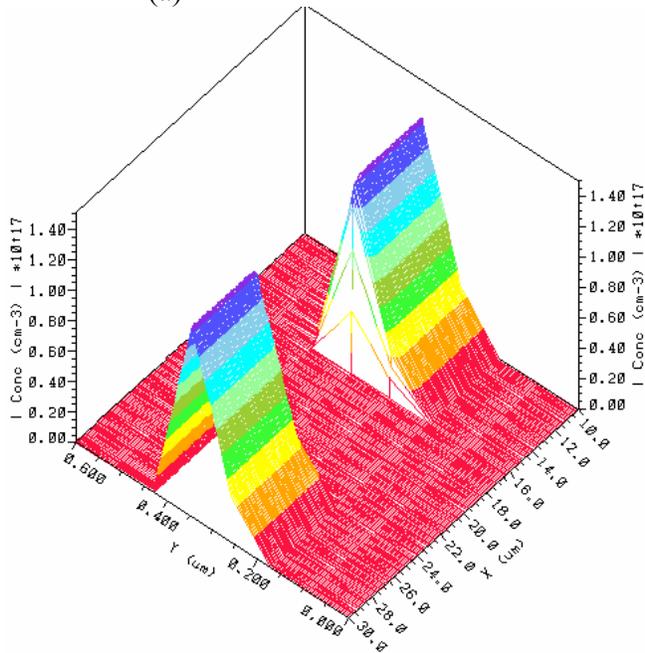


Figure 4.13: Trap occupation across device channel for MESFET with only source/drain residual implant damage traps. Note the absence of traps due to lateral straggle compared to the situation in Figure 4.8.

Figure 4.14 further shows the 3-D trap occupation (unoccupied trap distribution) at  $V_{DS} = 19 \text{ V}$  on the forward and return curves for  $V_{GS} = -20 \text{ V}$ . Again, the trap occupation is the same for the forward and return curves. The regions of trap occupation due to the lateral straggle of implanted species are absent compared to the situation depicted in Figure 4.11. Figure 4.15 indicates that the 3-D current distribution at  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  is the same for both the forward and return curves leading to the absence of hysteresis in the drain I-V characteristics. This is due to the absence of capture and emission processes that take place in the volume of traps due to the damage created by the lateral straggle of implanted species, as already observed above.

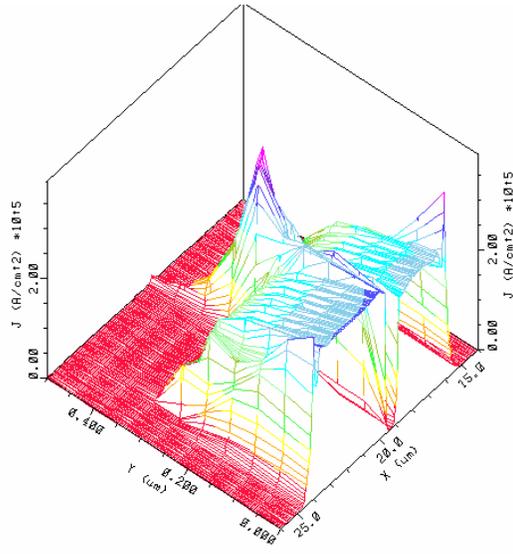


(a)

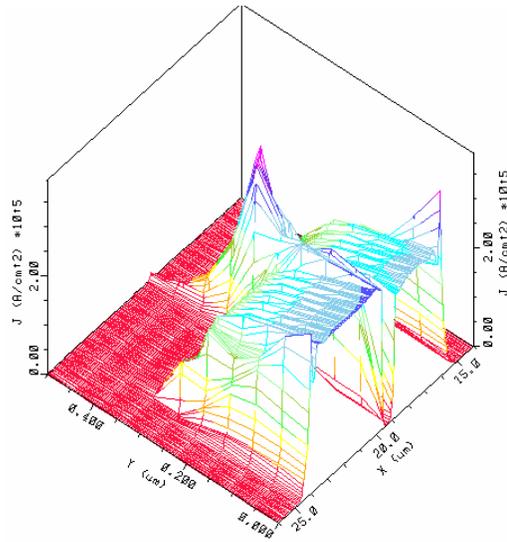


(b)

Figure 4.14: 3-D trap occupation (empty, unoccupied trap centers) for MESFET with only source/drain residual implant damage traps, without traps generated by lateral straggle of implanted ions at  $V_{DS}=19$  V,  $V_{GS} = -20$  V for (a) forward curve and (b) return curve. Note the absence of traps due lateral straggle compared to Figure 4.11.



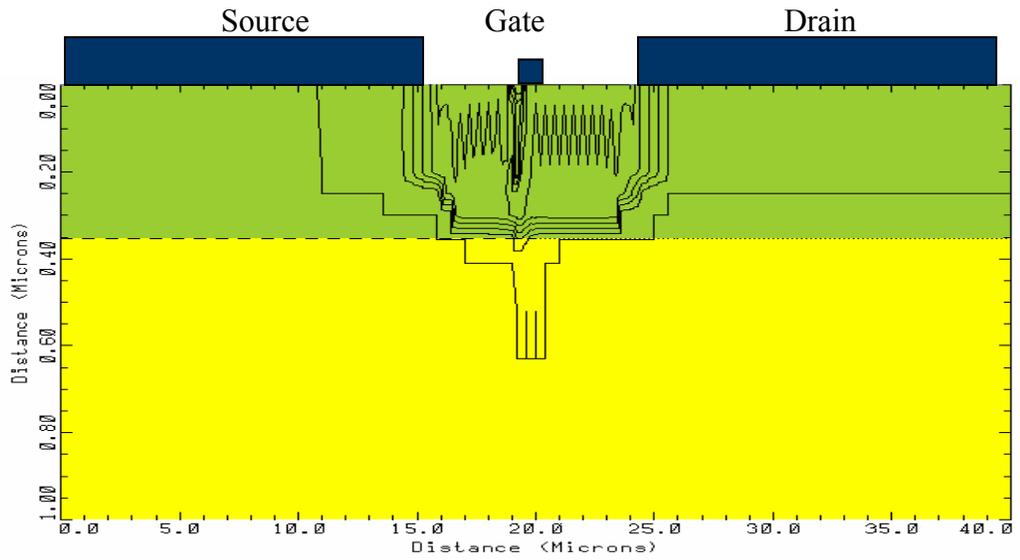
(a)



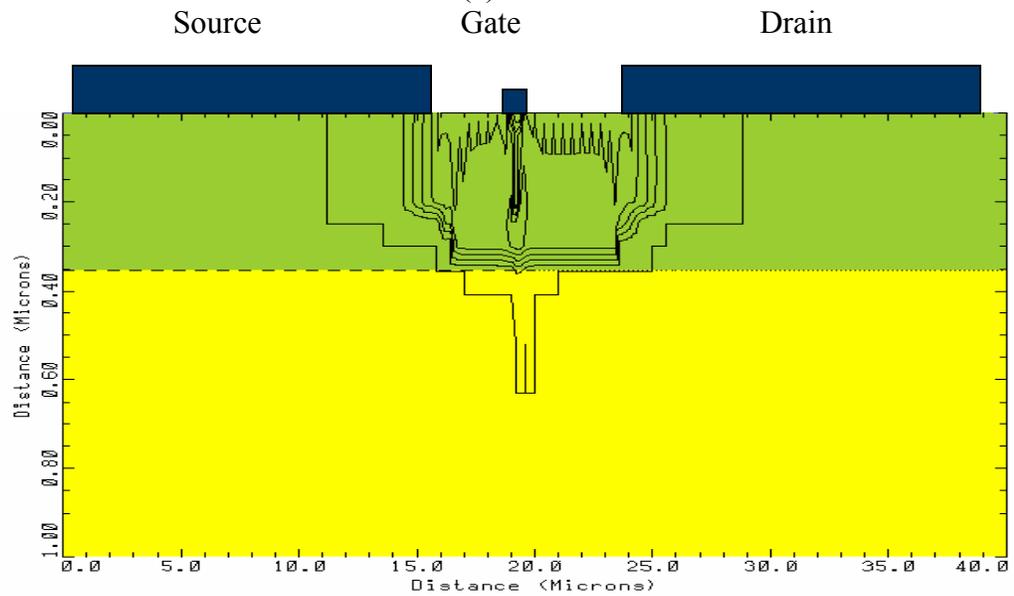
(b)

Figure 4.15: 3-D current distribution for MESFET with only source/drain residual implant damage traps, without traps generated by lateral straggle of implanted ions at  $V_{DS}=19$  V,  $V_{GS} = -20$  V for (a) forward curve and (b) return curve. Note that the current distributions are the same for the forward and return curves, hence no hysteresis occurs in the drain I-V curves.

The fact that the trapping and de-trapping occurs mainly in the volume of traps generated by the implant lattice damage due to the lateral straggle of implanted ions at un-gated regions of the inside edges of the source and drain is because, outside of the depleted region directly under the gate, the current mainly flows between the right edge of the source and left edge of the drain in the channel, as shown in Figure 4.16. Figures 4.17a and 4.17b show the 3-D current plots, which in addition to the plots in Figure 4.15 also confirm that the current flow is mainly restricted to the channel in the region between the inside edges of the source and drain. This is the location of the lateral straggle, causing the simulated hysteresis in the drain I-V curves.



(a)



(b)

Figure 4.16: 2-D Current contours for MESFET only source/drain residual implant damage traps at  $V_{DS}=19$  V for (a) forward curve (b) return curve.  $V_{GS} = -20$  V.

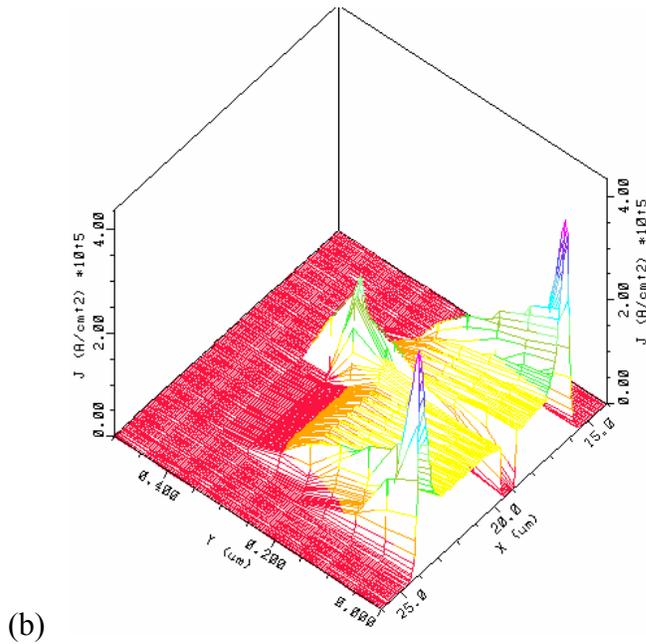
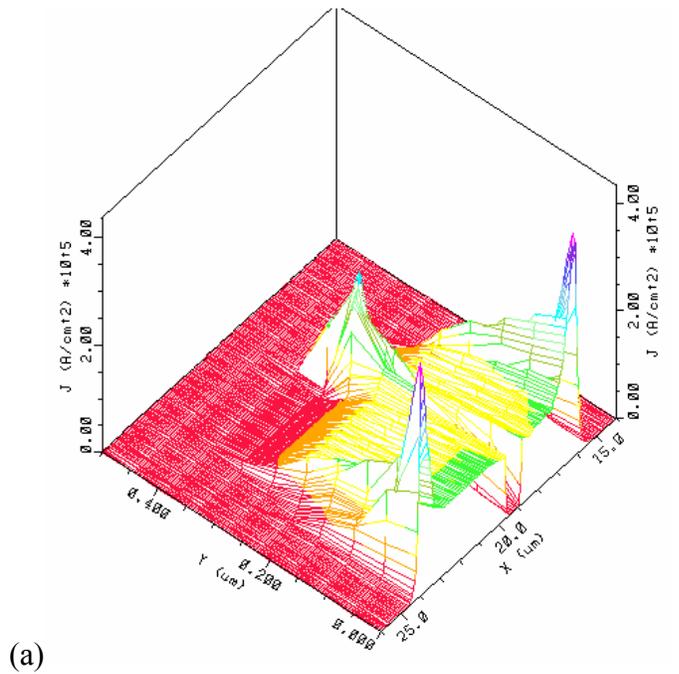
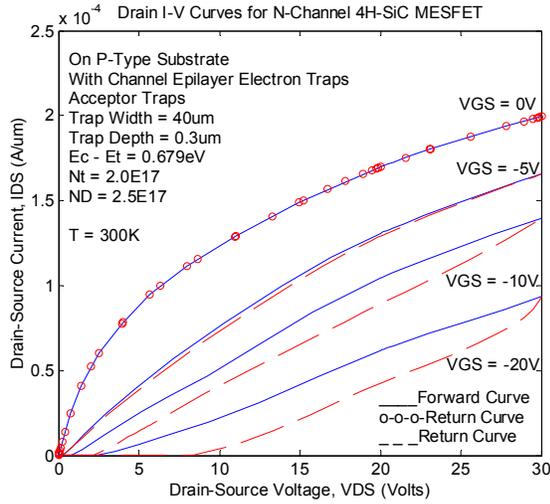


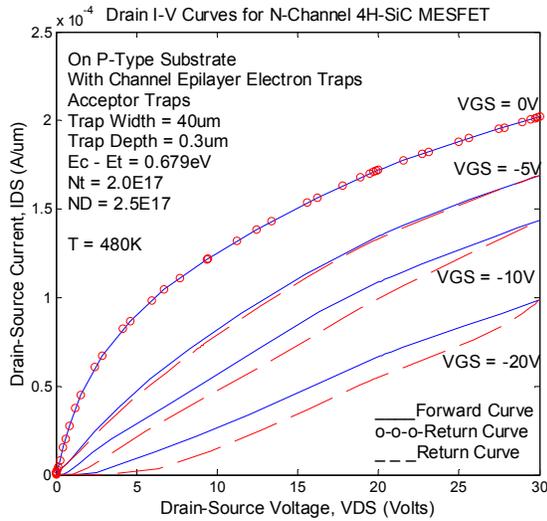
Figure 4.17: 3-D Current plots for MESFET with only source/drain residual implant damage traps at  $V_{DS}=19$  V for (a) forward curve. Note the presence of green patches. (b) return curve. Note the reduction of green patches. This is an indication of lower current.  $V_{GS} = -20$  V.

Figures 4.18a and 4.18b below show that if the channel traps are uniformly distributed spatially throughout the device channel, the hysteresis in the drain I-V characteristics increase with increasing negative  $V_{GS}$ , just as it occurs in the drain I-V characteristics of a MESFET with only SI substrate traps. However, as shown in Figure 4.18b, the hysteresis in the I-V curves of a MESFET with uniformly, spatially distributed channel traps does not disappear at 480 K as it does in the case of a MESFET with only SI substrate traps, although it appears reduced, particularly at high negative  $V_{GS}$  due to thermal emission of trapped electrons from trap centers. This is because the channel electrons are always in intimate contact with the channel traps, unlike in the case of SI substrate traps, where by the hysteresis in the I-V curves occurs due to trapping and emission processes at the channel-substrate interface for devices without p-buffer and buffer-substrate interface for devices with p-buffer layer through backgating effect, as discussed in Appendix A. Thus it appears that, it is only if the channel traps are locally restricted to the source and drain lateral straggle areas that hysteresis in the drain I-V characteristics of the MESFETs decreases with increasing negative  $V_{GS}$  as shown and discussed above, and depicted in Figures 4.7 to 4.11. As discussed above and in Appendix B, simulations suggest that it does not matter whether the channel traps are restricted to the source and drain lateral straggle areas or uniformly distributed over the source and drain ohmic contact regions and their attendant lateral straggle extensions, the hysteresis in the drain I-V curves appears to the same degree. Since the hysteresis in the drain I-V characteristics of the experimental MESFETs also generally decrease with increasing negative  $V_{GS}$ , particularly at 480 K as shown in Figures 3.1 3.2., it can be

inferred that the hysteresis in the experimental drain I-V characteristics could be attributed to source/drain residual implant lattice damage traps localized in the lateral straggle regions.



(a)



(b)

Figure 4.18: Simulated drain I-V characteristics of MESFET with channel epilayer traps uniformly distributed spatially in the channel at (c) 300 K (d) 480 K.

#### 4.4 Physics of Hysteresis – A Brief Survey

This section briefly discusses qualitatively the physics behind the hysteresis that appears in the drain I-V curves of MESFETs as it applies to source/drain implant damage traps. Appendix A gives a full survey of the hysteresis due to both source/drain implant damage traps and substrate traps. Using a single level trap with an energy level of  $E_C - 1.545$  eV obtained by Dalibor et al. after  $\text{He}^+$ -implantation [8], a MESFET on p-type substrate was simulated with trap concentration of  $1.8 \times 10^{17} \text{ cm}^{-3}$  and symmetric triangular pulse of 30 V amplitude and 30 s pulse width. Figure 4.19 shows the drain I-V characteristics and the band diagrams along lateral straggle regions on the source and drain sides at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$ ;  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$ ;  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ .

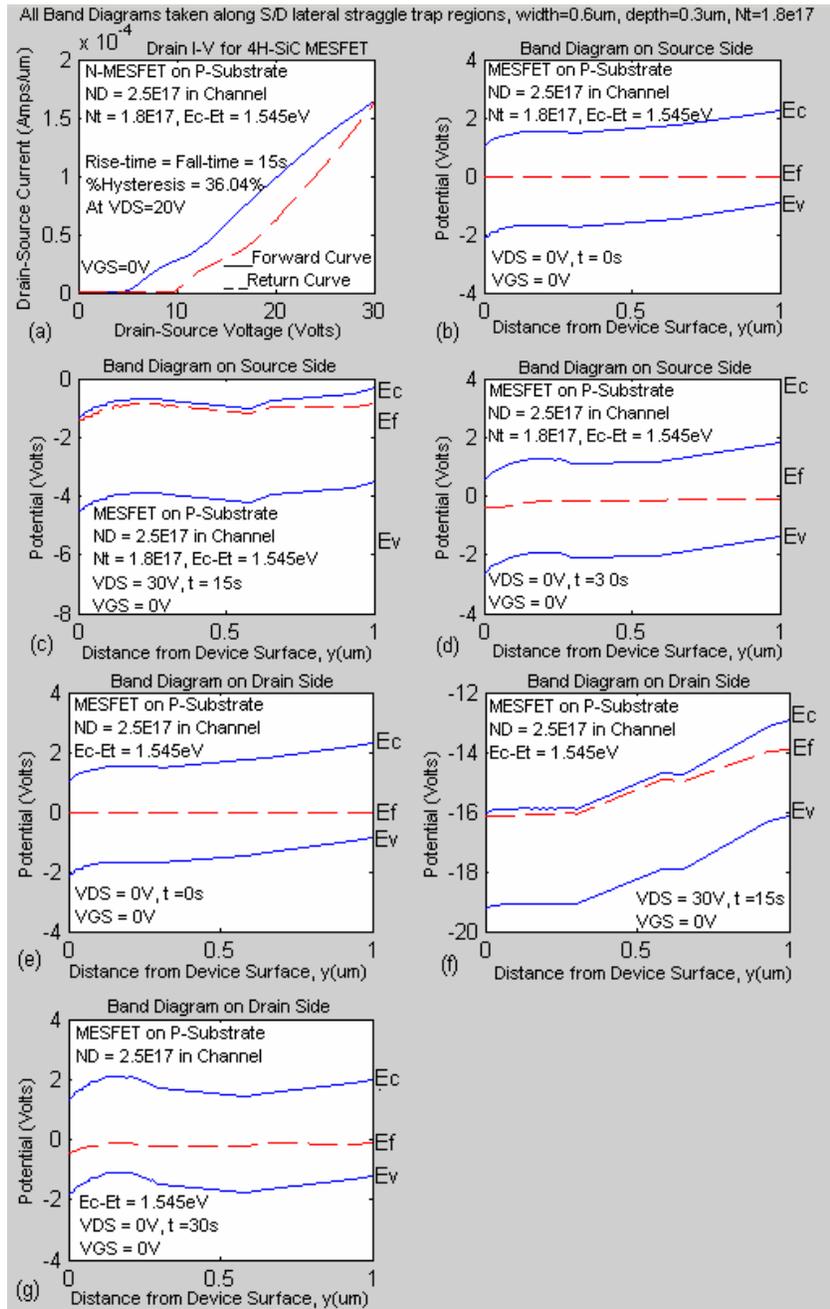


Figure 4.19: (a) Simulated drain I-V curves for 4H-SiC MESFET at  $V_{GS}=0$  V. Band diagram at source side for (b)  $V_{DS} = 0$  V,  $t = 0$  s (c)  $V_{DS} = 30$  V,  $t = 15$  s (d)  $V_{DS} = 0$  V,  $t = 30$  s. Band diagram at drain side for (e)  $V_{DS} = 0$  V,  $t = 0$  s (f)  $V_{DS} = 30$  V,  $t = 15$  s (g)  $V_{DS} = 0$  V,  $t = 30$  s.

The band diagrams at both the source and drain sides indicate that at  $V_{DS} = 0$  V,  $t = 0$  s the material is highly compensated as indicated by the position of the Fermi level,  $E_F$  due to electron capture and as discussed in Chapter I, section 1.3, by Hallen et al. [24] and Svensson et al. for an implanted SiC material. At  $V_{DS} = 30$  V,  $t = 15$  s, however, due to the emission-dominant process as  $V_{DS}$  rises from 0 V to 30 V the material becomes highly n-type since the Fermi level,  $E_F$  is very close the conduction band edge,  $E_C$ . At  $V_{DS} = 0$  V,  $t = 30$  s due to the electron capture-dominant process as  $V_{DS}$  falls from 30 V to 0 V, the material becomes highly compensated again as indicated by the position the Fermi level,  $E_F$ . Comparing Figures 4.19 (d) and 4.19 (g) it can be seen that the material is more compensated at the drain side than at the source side, indicating that there are more trapped electrons at drain side than at the source side. This is due to the high electric fields at the drain side, which injects more electrons into trap centers. This suggests that much of the hysteresis in the drain I-V curves is due to capture and emission processes at the drain side as will be shown later and discussed in Appendix A.

Figures 4.20 show the band diagrams at  $V_{DS} = 20$  V for the forward and return curves and the corresponding empty trap density and free electron concentration taken along the lateral straggle regions at the source and drain sides. As usual, the empty trap density on the return curves is less than that on the forward curves, indicating that more free electrons are trapped as  $V_{DS}$  falls from  $V_{DS(max)} = 30$  V to 0 V. This is confirmed by the corresponding electron density plots in Figures 4.20 (e) and (f), which are lower on the return curves than on the forward curves due to the dominant electron capture process.

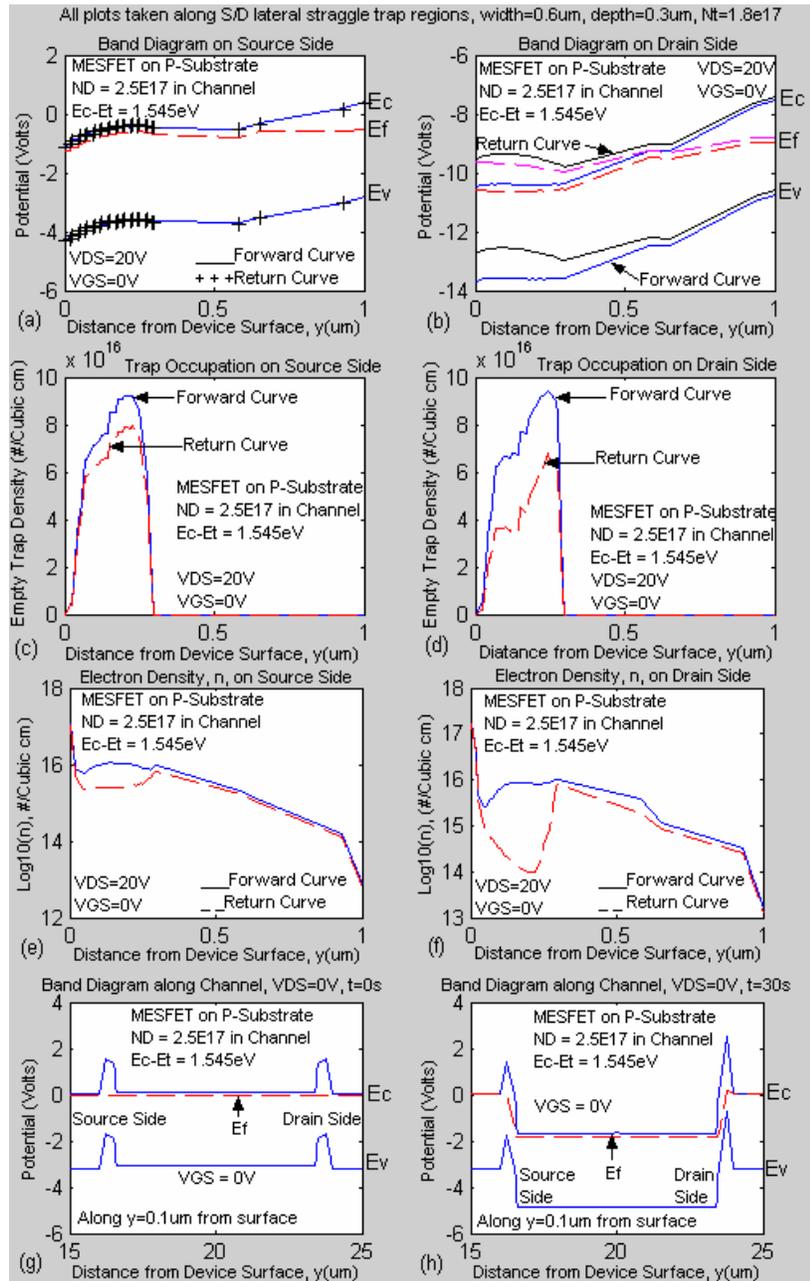


Figure 4.20: Band diagram for 4H-SiC MESFET with single level trap at  $V_{DS} = 20$  V at (a) source side (b) drain side, corresponding trap occupation at (c) source side and (d) drain side. Free electron density along lateral straggle regions at (e) source side (f) drain side. Band diagram along channel at (g)  $V_{DS} = 0$  V,  $t = 0$  s (h)  $V_{DS} = 0$  V,  $t = 30$  s.

Figure 4.20(b) shows that on the return curve as  $V_{DS}$  falls due to the electron capture-dominant process, the potential due to trapped electrons is higher than on the forward curve where electron emission dominates. As a result the unoccupied trap density is lower on the return curve than on the forward curve with a corresponding lower free electron concentration on the return curve than on the forward curve, giving rise to the hysteresis in the drain I-V curves. The band diagrams further show that there is more band bending on the return curve at the drain side than at the source side, suggesting that more electron trapping occurs at the drain side than at the source side as already mentioned elsewhere above. This is also borne out by the trap occupation plots and electron density plots, which show larger difference between the forward and return curves at the drain side than at the source side.

The band diagram across the channel at a distance of  $0.1 \mu\text{m}$  from the device surface show that at  $t = 0 \text{ s}$  the potential barrier due to trapped electrons is about the same at the source and drain sides. At  $t = 30 \text{ s}$ , however, due to excessive electron trapping at the drain side as  $V_{DS}$  falls back to  $0 \text{ V}$ , the potential barrier at the drain side is higher than that at the source side. This indicates that much of the hysteresis in the drain I-V characteristics is due to trapping and emission processes at the drain side as a result of the high electric fields at the drain region as already mentioned.

#### 4.5 Simulation of MESFET with Implant Damage Traps Obtained from the Literature

In this section the simulations of a MESFET with implant damage traps obtained from the literature are used to represent the source/drain residual implant lattice damage. The simulation device is constructed on p-type conductive substrate with traps simulating only source/drain implant damage and no SI substrate traps. In particular, implant damage traps generated by implanting n-type 4H-SiC CVD epilayers with  $\text{He}^+$ ,  $\text{Ti}^+$ , and  $\text{V}^+$  performed by Dalibor et al. [8], and implant damage traps generated by implanting n-type 4H-SiC samples with  $\text{Al}^+$  and  $\text{B}^+$  performed by Troffer et al. [9] are considered. Figure 4.21 shows the simulated drain I-V characteristics for a MESFET for which the traps generated by  $\text{He}^+$ -implantation of n-type 4H-SiC CVD epitaxial layers shown in Figure 1.6 and Table 1.1 obtained by Dalibor et al. [8] are used for the source/drain implant damage traps.

Figure 4.22 below depicts the simulated drain I-V characteristics of a MESFET in which the traps generated by the  $\text{Ti}^+$ - or  $\text{V}^+$ -implantation of n-type 4H-SiC CVD epilayers obtained by Dalibor et al. [8] and shown in Figure 1.7 and Table 1.2 are used for the source/drain implant damage traps. It should be noted that the same set of traps are generated by both the  $\text{Ti}^+$ - and  $\text{V}^+$ -implantations and are not related to either Ti or V. The traps are therefore implant species independent as already mentioned in Chapter I.

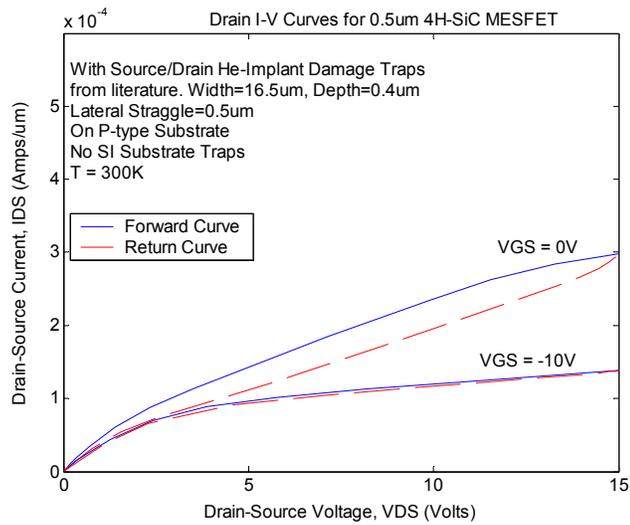


Figure 4.21: Simulated drain I-V curves for MESFET in which, traps generated by  $\text{He}^+$ -implantation of n-type 4H-SiC epilayers as observed by Dalibor et al. [8] are used for the source/drain implant damage traps.

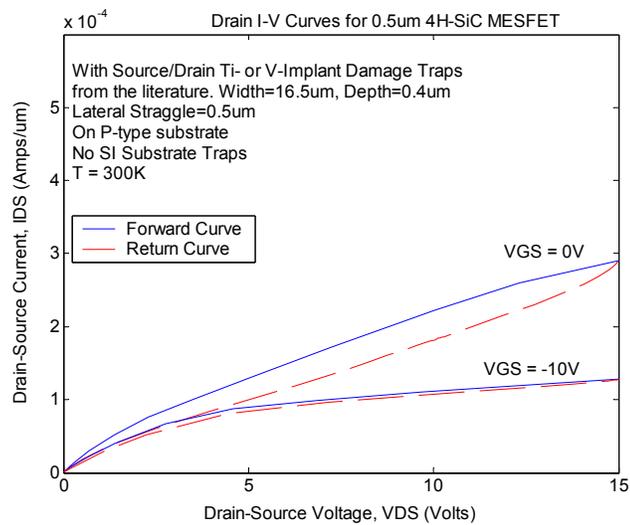


Figure 4.22: Simulated drain I-V curves for MESFET in which, traps generated by  $\text{Ti}^+$ - or  $\text{V}^+$ -implantation of n-type 4H-SiC epilayers detected by Dalibor et al. [8] are used for the source/drain implant damage traps.

In Figure 4.23 is shown the simulated drain I-V curves for a MESFET in which traps generated by implanting n-type 4H-SiC with Al<sup>+</sup> performed by Troffer et al. [9], and shown in Figure 1.11 and Table 1.5 are used for the source/drain implant damage traps only and no SI substrate traps. Also Figure 4.24 shows the simulated drain I-V characteristics for a MESFET for the case in which the traps used for the source/drain implant damage traps are those generated by implanting n-type 4H-SiC samples with B<sup>+</sup> obtained by Troffer et al. [9] and shown in Figure 1.11 and Table 1.6. Again, no SI substrate traps are included in the simulation. As already observed Chapter I, the same traps generated by implanting n-type 4H-SiC samples with Al<sup>+</sup> and B<sup>+</sup> are also observed by Dalibor et al. [8] after implanting n-type 4H-SiC epilayers with Ti<sup>+</sup> or V<sup>+</sup>. As such these traps are not implant species dependent and are therefore intrinsic defects, which could be possibly generated by implantation of n-type 4H-SiC samples by other dopants such as nitrogen (N) and any high-energy particle irradiation of the 4H-SiC material. As already indicated in Chapter I, section 1.3, Dalibor et al. [8] have established that these implant damage traps are acceptor-like.

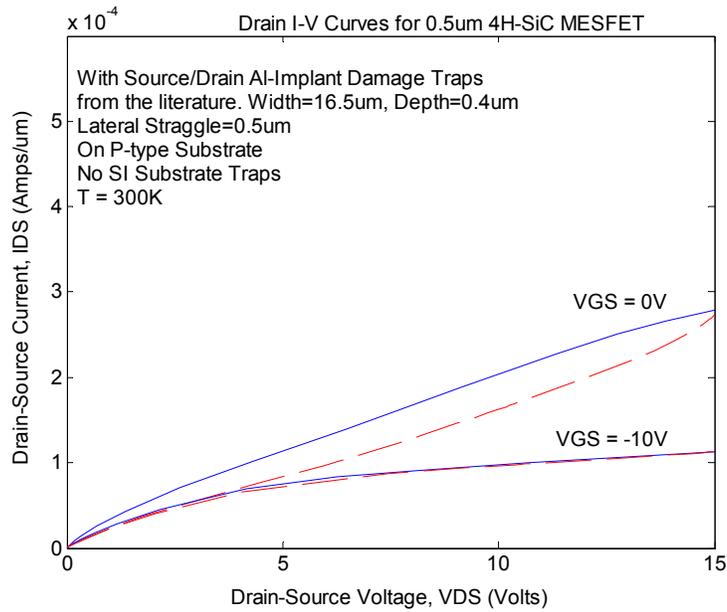


Figure 4.23: Simulated drain I-V curves for MESFET in which, traps generated by Al<sup>+</sup>-implantation of n-type 4H-SiC samples obtained by Troffer et al. [9] are used for the source/drain implant damage traps.

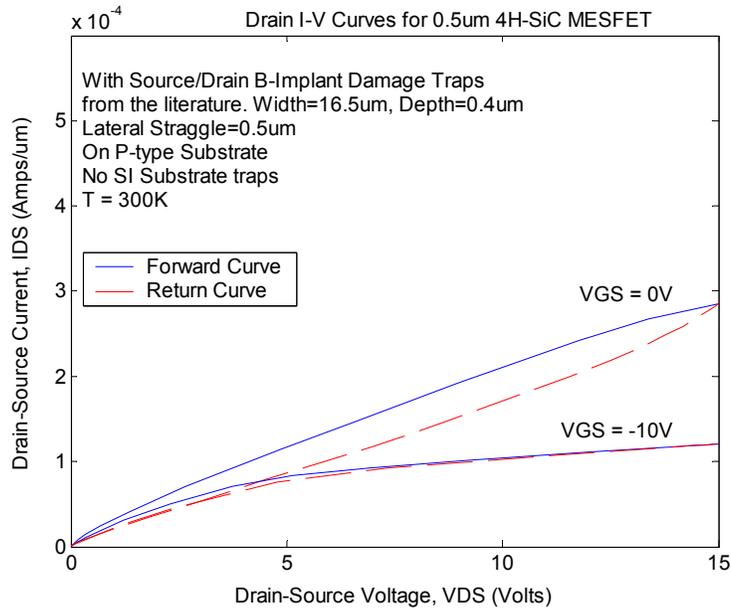


Figure 4.24: Simulated drain I-V curves for MESFET in which, traps generated by B<sup>+</sup>-implantation of n-type 4H-SiC samples obtained by Troffer et al. [9] are used for the source/drain implant damage traps.

The above results serve to confirm our hypothesis that source/drain residual implant damage traps and residual implant damage traps in general could generate hysteresis in the drain I-V characteristics of MESFETs and FETs in general. It is interesting to note from Figure 4.21 to Figure 4.24 that the degree of hysteresis in the drain I-V is about the same for all four diagrams, indicating that the four set of traps may have similar characteristics. In addition the drain current levels are about the same. It can also be seen that the hysteresis at  $V_{GS} = -10$  V is very much reduced in contrast with the simulated drain I-V curves shown in Figure 4.7 in which the source/drain residual implant damage traps are energetically distributed throughout the 4H-SiC band gap. This could be due to the fact that the traps used for the simulated drain I-V curves in Figures 4.21 to 4.24 are restricted to the upper half of the 4H-SiC band gap and have specific energy levels as shown in Tables 1.3, 1.6, and 1.7.

## CHAPTER V

### OPTICAL ADMITTANCE SPECTROSCOPY MEASUREMENTS

#### 5.1 Underlying Concepts of Thermal and Optical Admittance Spectroscopy

Shallow impurities and shallow level defect trap centers can be studied by thermal admittance spectroscopy (TAS), and other traditional thermal spectroscopic measurement techniques, such as Hall Effect measurements and deep level transient spectroscopy (DLTS). These measurement techniques can also be used to investigate deep level defect trap centers in narrow band gap semiconductors such as silicon. The principle of thermal admittance spectroscopy (TAS) is based on the fact that when a junction diode or Schottky diode that contains a defect level in the band-gap is modulated with a small sinusoidal signal of frequency  $\omega$  and amplitude  $\delta V$ , an additional capacitance  $C_T$  and conductance  $G_T$  arise from the emission of carriers excited from the defect center [35, 60, 61, 62]. The excitation occurs as the sinusoidal signal modulates the defect level past the Fermi level via band bending [35, 60, 61, 62]. The TAS measurement technique is thus based on the variations of the junction capacitance and conductance as a function of temperature and measurement signal frequency.

Figure 5.1 shows a sketch of the energy band diagram of a reverse biased Schottky diode for n-type material with a trap energy level  $E_t$  in the upper half of the band gap.  $V_d$  is diode built-in voltage,  $V_r$  is the applied reverse bias,  $E_d$  is the donor level,  $E_f$  is the Fermi level, and  $E_C$  and  $E_V$  are the conduction and valence bands respectively.

$X_0$  is the depletion region width and  $X$  is the point of intersection of  $E_t$  and  $E_f$ . Since an applied AC voltage also modulates the space charge region width, the capacitance  $C_T$  and conductance  $G_T$  measurements of the diode can also be viewed as being based on the modulation of the width of the depletion region by the applied sinusoidal (AC) voltage of frequency  $\omega$  and amplitude  $\delta V$  [61].

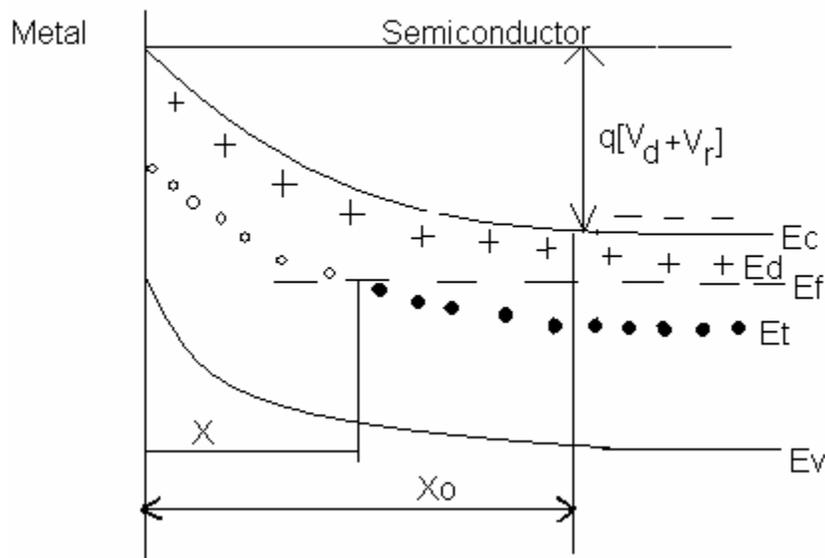


Figure 5.1: Energy band diagram of a Schottky barrier diode on n-type material.

When the applied voltage is changed from  $V_r$  to  $V_r + \delta V$ , the crossing point of  $E_f$  and  $E_t$  (the  $X$  point) moves from  $X$  to  $(X + \delta X)$  and the traps, which are above the Fermi level emit their electrons into the conduction band with emission rate  $e_n$  and those below the Fermi level will be filled with electrons [62]. When the applied reverse bias voltage is decreased by  $\delta V$  (i.e.  $V_r - \delta V$ ), the intersection point of  $E_f$  and  $E_t$  moves from  $X$  to  $(X - \delta X)$  and more electrons are then trapped. The trapping and emission of electrons from trap levels and modulation of the depletion region width, during the excursions of the

measurement AC signal voltage, together lead to variations in the junction capacitance and conductance of a diode (Schottky or diffused), and these give rise to the underlying principles of admittance spectroscopy in general.

The study of deep defect levels near mid-gap in wide band gap semiconductors such as SiC by thermal spectroscopic means is made more difficult because of the high temperatures required to move the Fermi level to near mid-gap in order to detect such traps [35, 60]. Optical admittance spectroscopy (OAS), a variation of TAS, is a more suitable method for investigating deep defect levels such as those near mid-gap in SiC without using very high temperatures. OAS like TAS is used to measure various parameters of deep level traps in junctions such as activation energy, capture cross section, and concentration. The OAS measurement technique is also based on variations of junction capacitance  $C_T$  and conductance  $G_T$ , but in this case of a junction under illumination, as a function of photon energy  $h\nu$  at a constant measurement signal frequency and temperature [35, 60, 61, 62].

The additional diode conductance  $G_T$  introduced by the presence of traps is given by [35, 62]

$$G_T = A \left( \frac{e_n \omega^2}{e_n^2 + \omega^2} \right) \frac{N_T}{n} \left( \frac{q\varepsilon N_+}{2(V_r + V_d)} \right)^{1/2} \quad (5.1)$$

The exchange of electrons between the traps and the conduction band also lead to an additional capacitance  $C_T$ , which is given by [35, 62]

$$C_T = A \left( \frac{e_n^2}{e_n^2 + \omega^2} \right) \frac{N_T}{n} \left( \frac{q\varepsilon N_+}{2(V_r + V_d)} \right)^{1/2} \quad (5.2)$$

where  $A$  is the diode area,  $N_+$  is the fixed charge density in the depletion region,  $\epsilon$  is the dielectric constant of the material,  $\omega$  is the sinusoidal signal measurement frequency,  $n$  is the free electron concentration,  $N_T$  is the trap concentration,  $V_d$  is the diode or junction built-in voltage,  $V_r$  is the applied reverse bias which is usually zero, and  $e_n$  is the thermal emission rate from defect levels. The quantities  $N_+$ ,  $N_T$ ,  $n$ , and  $e_n$  are expected to vary with temperature [62]. The dependence of the thermal emission rate  $e_n$  on temperature can be expressed as [54, 79]

$$e_n = \sigma \langle v_{th} \rangle N_C \exp\left(-\frac{E_C - E_T}{kT}\right) \quad (5.3)$$

where  $\sigma$  is the capture cross section of the defect center,  $\langle v_{th} \rangle$  is the average thermal velocity of electrons, and  $N_C$  is the effective density of states in the conduction band and can be expressed as

$$N_C = 2 M_C \left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \quad (5.4)$$

$M_C$  is the number of equivalent conduction band minima,  $m^*$  is the effective mass for electrons,  $k$  is Boltzmann's constant, and  $h$  is Planck's constant. It can be seen from equations 5.1-5.4 that the temperature dependence of  $G_T$  and  $C_T$  is primarily determined by the emission rate,  $e_n$  [35].

Figures 5.2(a-c) [61], show the variations of  $C_T$  and  $G_T$  with sinusoidal measurement signal frequency  $\omega$ , temperature  $T$ , and photon energy  $h\nu$ , respectively. As reported in the literature,  $C_T(\omega)$  and  $G_T(\omega)$  plots of a junction with a deep level show an inflection point [61, 62]. In Figure 5.2(a), according to Duenas [61], the variations of

$C_T(\omega)$  and  $G_T(\omega)$  are due to the change in the measuring signal frequency with respect to the time constant of the charge and discharge processes of the deep level around the point of intersection of  $E_f$  and  $E_t$ . When  $\omega \ll e_n^t$ , the  $C_T$  and  $G_T$  measured are those of low frequency and the modulation of the depletion region occurs at its edge and at the intersection of  $E_f$  and  $E_t$  [61]. At low frequency the measured conductance  $G_T$  approaches zero, since conductance is proportional to the measurement frequency ( $G_T \propto \omega$ ) and the measured capacitance is a parallel combination of the capacitance due to the depletion region and that due to trapped charge, which results in the measured capacitance being a maximum. When  $\omega \gg e_n^t$ , the  $C_T$  and  $G_T$  measured are those of high frequency, and the space charge region (SCR) modulation occurs only at its edge [61] since the SCR due to trapped charge cannot respond to  $\omega$ .

The measured capacitance is that of the depletion region only which is minimum and the measured conductance, is maximum since  $G \propto \omega$ . The low frequency to high frequency transitions in  $C_T$  and  $G_T$  occur when  $\omega \approx e_n^t$  and both  $C_T(\omega)$  and  $G_T(\omega)$  plots show an inflection point [61].

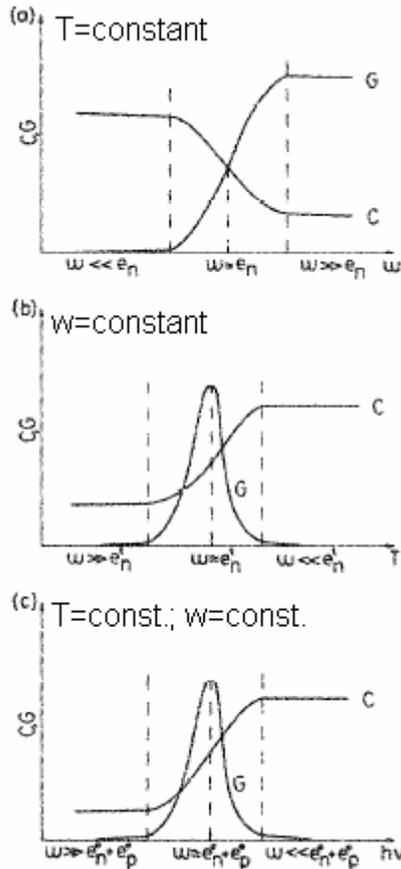


Figure 5.2: (a) Capacitance and conductance versus AC measurement frequency at constant temperature (b) Capacitance and conductance versus temperature at constant AC signal measurement frequency (c) Capacitance and conductance versus photon energy at constant temperature and measurement frequency [61].

From Figure 5.2(b), due to the same physical processes as described above, at a constant frequency  $\omega$  the  $C_T(T)$  plot shows a point of inflection and the  $G_T(T)$  plot shows a maximum at a temperature  $T_i$  or  $T_m$  when  $\omega \approx e_n^t$  [35, 61, 62]. At low temperatures,  $\omega \gg e_n^t$  and the measured  $C_T$  and  $G_T$  are those of high frequency and at high temperatures,  $\omega \ll e_n^t$  and the measured  $C_T$  and  $G_T$  are those of low frequency [35, 61]. The maximum in  $G_T(T)$  occurs because the conductance is proportional to the thermal emission rate of electrons ( $G \propto e_n^t$ ), and at low temperatures, although the conductance is that of high

frequency, its value vanishes since  $e_n^t$  approaches zero ( $e_n^t \cong 0$ ) [61]. Duenas et al. [61] therefore define thermal admittance spectroscopy (TAS) as a technique that allows the thermal emission rates of carriers to be measured from  $C_T(T)$  and  $G_T(T)$  plots at a constant measurement frequency.

When the capacitance  $C_T$  and conductance  $G_T$  of a junction with a deep level trap, under optical illumination, at constant temperature and measurement signal frequency, are plotted as a function of photon energy  $h\nu$ , the  $C_T(h\nu)$  curve will show an inflection point and the  $G_T(h\nu)$  curve will indicate a maximum when  $\omega \cong e_n^o + e_p^o$ , as shown in Figure 5.2(c) [61]. Here,  $e_n^o$  and  $e_p^o$  are the optical emission rate of electrons and holes respectively, from trap levels. According to Duenas et al. [61], these capacitance and conductance variations are due to the change that the time constant of the charge and discharge processes of the deep level experiences around the point of intersection of  $E_f$  and  $E_t$  under illumination, with respect to the measuring signal frequency. At a temperature such that  $e_n^o + e_p^o \gg e_n^t$ , when the photon energy is such that  $\omega \gg e_n^o(h\nu) + e_p^o(h\nu)$ , the high frequency values of  $C_T$  and  $G_T$  will be measured and when  $\omega \ll e_n^o(h\nu) + e_p^o(h\nu)$  the low frequency values will be measured [61]. It can be observed from Figure 5.2(c) that, the  $G_T(h\nu)$  has a maximum because the conductance is proportional to  $e_n^o(h\nu) + e_p^o(h\nu)$ , and at low photon energy, although the conductance is that of high measurement frequency, its value vanishes ( $G_T(h\nu) \cong 0$ ) since  $e_n^o(h\nu) + e_p^o(h\nu) \cong 0$  [61]. This is due to the fact that conductance is proportional to the free carrier concentrations ( $n$  and  $p$ ) which are in turn proportional to the optical emission rates ( $e_n^o$  and  $e_p^o$ ). Thus at

low photon energy ( $h\nu$ ) the emission rates are nearly zero and hence the conductance vanishes, resulting in the maximum point in the conductance curve.

If the temperature of the sample under investigation is lowered to a point where thermal emission of carriers is minimum, i.e.  $e_n^t \ll \omega$  and/or  $e_n^t \ll e_n^o + e_p^o$ , carriers may be excited from defect levels within the band-gap to the respective energy bands ( $E_C$  and/or  $E_V$ ) by illuminating the sample with monochromatic light of a wavelength such that the energy of the photon is equal to (or greater than) the transition energy from the defect level to the respective band edge [35]. In the case of donors (or ionized acceptors) in an n-type material an electron is excited from the defect center to the conduction band and in a p-type material, an electron is excited from the valence band to the defect level and a hole is left behind in the valence band [35], which is equivalent to a hole being ejected from the defect level to the valence band. In both cases, the carriers excited to their respective bands move to the edge of the depletion region where they are detected by the change in the capacitance and conductance. According to Smith et al. [35], intra-center and by extension inter-center transitions will not be seen, since a change in net carrier density at the depletion region edge is required to change  $C_T$  and  $G_T$ . This, according to Smith et al., is the principle of Optical Admittance Spectroscopy (OAS), which was introduced by Vincent et al. [62] and later developed by Duenas et al. [61]. Using OAS measurements, it is possible to investigate deep levels in wide band gap semiconductors such as SiC without resorting to the high temperatures required to move the Fermi level to mid-gap in such measurements as Hall effect, DLTS [54] and TAS, as already mentioned elsewhere in this work. Smith et al. [35] point out that in OAS since the

thermal emission rate of electrons  $e'_n$  is negligible, from equations 5.1 and 5.2, the response of a diode with a deep level is directly determined by  $N_+$ . They further note that OAS gives the optical transition energy and not the thermal transition energy as in Hall effect, TAS, or DLTS measurements.

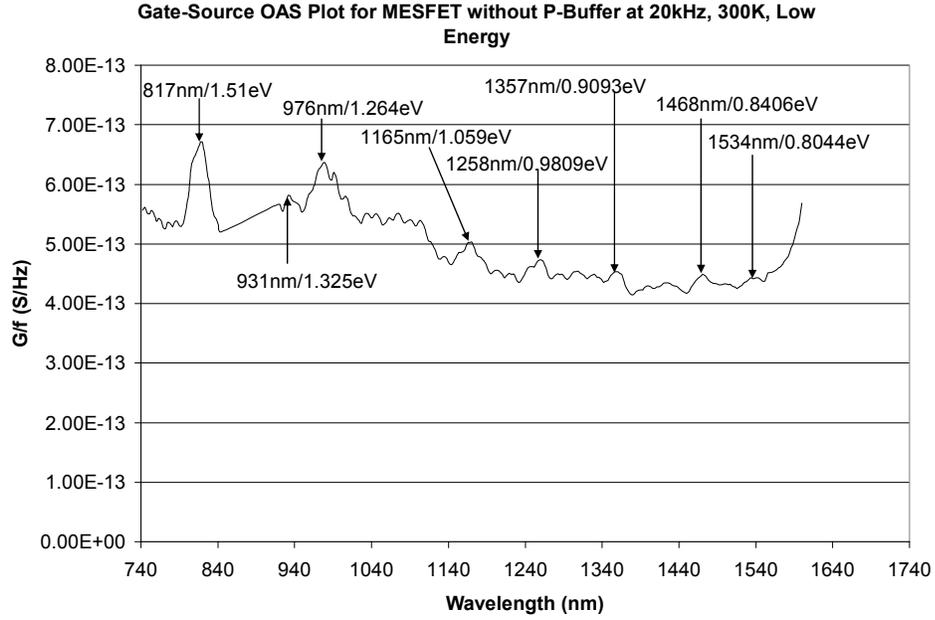
It can be seen from equations 5.1 and 5.2 that both the conductance and capacitance depend on  $(N_+)^{1/2}$ . Vincent et al. [62] therefore point out that if  $N_+$  is affected by illumination of the barrier (junction), the conductance must change in the same fashion as the capacitance, leading to a photo-conductance effect. The authors have shown that at low temperatures such as 77 K where photoconductivity is high, the photo-conductance and photo-capacitance spectra have similar shape due to their dependence on  $N_+$ , which is confirmed by other authors [35, 63]. It is important to note that for optical detection of deep levels, it is necessary to lower the sample temperature to a temperature such that the thermal emission of carriers is negligible so that photoemission of carriers from deep levels can be detected [35, 60, 61, 62, 63]. OAS measurements are generally performed in the temperature range of about 40 K-300 K [35, 60, 61, 62, 63].

## **5.2 Results of Room Temperature (300 K) OAS measurements**

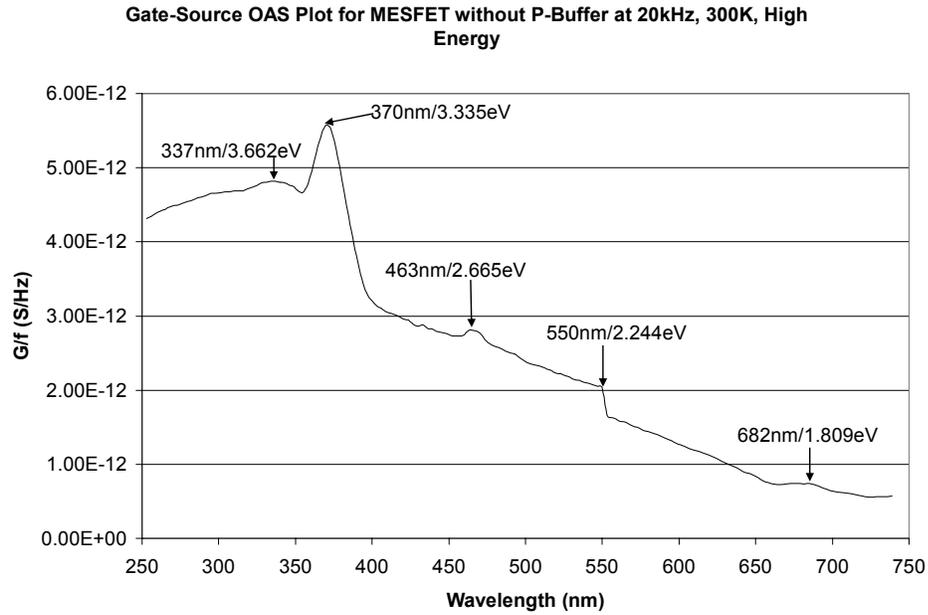
The optical admittance spectroscopy measurements were performed with an HP4284A multi-frequency LCR meter operated in the high-resolution mode at 20 kHz. The measurements were first made at 300 K (room temperature) and then at 200 K. A 450-1000 W Oriel Instruments Xenon arc lamp, model 6269, and an Oriel Monochromator Model 74100 provided the monochromatic light. The DC bias was set at

0 V and the AC measuring signal amplitude was 0.05 V. The devices used in the OAS measurements have two gates with gate periphery of 0.2 mm a microphotograph of which is shown in Figure 2.1.

Figure 5.3(a) depicts the gate-source optical admittance spectrum of an experimental MESFET without p-buffer layer obtained at 300 K using a 20 kHz AC measuring signal and long wavelength (low energy) optical signal and Figure 5.3(b) shows the short wavelength (high energy) spectrum. The gate-drain spectra are similar. Figures 5.4 (a) and (b) respectively show the low and high optical energy gate-drain OAS spectra for an experimental MESFET with p-buffer layer at 300 K. The gate-source spectra are also similar for this case. A comparison of the low energy (long wavelength) spectra for the both types of devices show several peaks in the spectrum of the device without p-buffer while the spectrum for the device with p-buffer shows practically no peaks except for the peak centered at about 817 nm with activation energy of  $E_C - 1.51$  eV, which is reduced relative to the corresponding peak in the spectrum of the device without buffer. This suggests that the observed peaks in the spectrum of the device without p-buffer layer are due largely to substrate traps and that the p-buffer layer is effective in isolating the channel from the substrate.



(a)



(b)

Figure 5.3: Gate-source OAS spectrum for experimental MESFET without p-buffer at 300 K for (a) long optical wavelength (b) short optical wavelength. Note: the gate-drain spectra are similar.

Comparing the high energy spectra of both types of devices (Figures 5.3(b) and 5.4(b)) it can be observed that the peak centered at about 370 nm with corresponding energy level of  $E_C - 3.335$  eV, which corresponds to the 4H-SiC band gap is much more pronounced in the spectrum of the device without p-buffer (Figure 5.3(b)) than in the spectrum of the device with p-buffer layer as shown in Figure 5.4b. Also the small peak centered at about 463 nm with activation energy of  $E_C - 2.665$  eV in the spectrum of the device without p-buffer (Figure 5.3(b)) completely vanishes in the Figure 5.4(b), which shows the high energy gate-drain OAS spectrum for the device with p-buffer layer. This further suggests that the peaks in the spectrum of device without p-buffer are due to substrate traps and further demonstrates the effectiveness of the p-buffer layer in isolating the channel from the substrate.

From Figures 5.3 (b) and 5.4 (b) it can be seen that the peak centered at about 682 nm with energy level of  $E_C - 1.809$  eV in the spectrum of the device without buffer completely disappears in the spectrum of the device with buffer, indicating that the 682 nm peak is due to substrate traps. This peak could be attributed to the vanadium donor level, which is known to be located close to mid-gap [53, 54, 55, 56, 57, 58, 60]. The inflections in Figures 5.3 (b) and 5.4 (b) at 550 nm are due to filter change and are not attributable to any traps. The broad peak in Figure 5.3 (b) centered at about 337 nm with activation energy of  $E_C - 3.662$  eV and the peak in Figure 5.4 (b) at about 271 nm with energy level of  $E_C - 4.553$  eV can be attributed to transitions from within the valence band to the conduction band and are not due to any band gap transitions, since the activation energies are greater than the 4H-SiC band gap.

It is interesting to note that the peak centered around 817 nm with activation energy of  $E_C - 1.51$  eV, which is observed in the spectra both types of devices although it is reduced in the spectrum of the device with buffer corresponds to a DLTS peak detected by T. Dalibor et al. [8] after  $\text{He}^+$ -implantation and anneal of n-type 4H-SiC CVD epilayers. Dalibor et al. [8] refer to this peak as  $\text{RD}_4$  and has an activation energy, which ranges from  $E_C - 1.49$  eV to  $E_C - 1.60$  eV as shown in Figures 1.6 and 1.9 and Table 1.1. The authors attribute this peak to an intrinsic defect due to residual implant lattice damage caused by the  $\text{He}^+$ -implantation of the n-type 4H-SiC CVD epilayers since it is not related to He. Thus this peak could be due to traps generated by ion-implantation and any high-energy particle bombardment of SiC layers. Furthermore, the broad nature of the 817 nm peaks and their associated peaks, which will be shown in subsequent figures, suggests that the traps responsible for these peaks have distributed energy levels. This observation is consistent with implant damage traps in general, since as shown in Chapter I, section 1.3, implant damage traps have energy levels distributed in the SiC bandgap [8, 9, 10, 11, and 24].

The fact that 817 nm peak is reduced in the spectrum of the device with buffer as shown in Figure 5.4(a) compared to the corresponding peak in the spectrum of the device without buffer (Figure 5.3(a)) can be explained by the realization that lattice implant damage can extend beyond the projected range by as much as twice the projected range as determined by Koshka et al. [13]. It is therefore quite plausible that the lattice implant damage in both types of devices extends beyond the channel into the substrate and that the p-buffer layer effectively screens the substrate portion of the residual implant lattice

damage traps in the devices with buffer, revealing only the channel portion as an OAS peak.

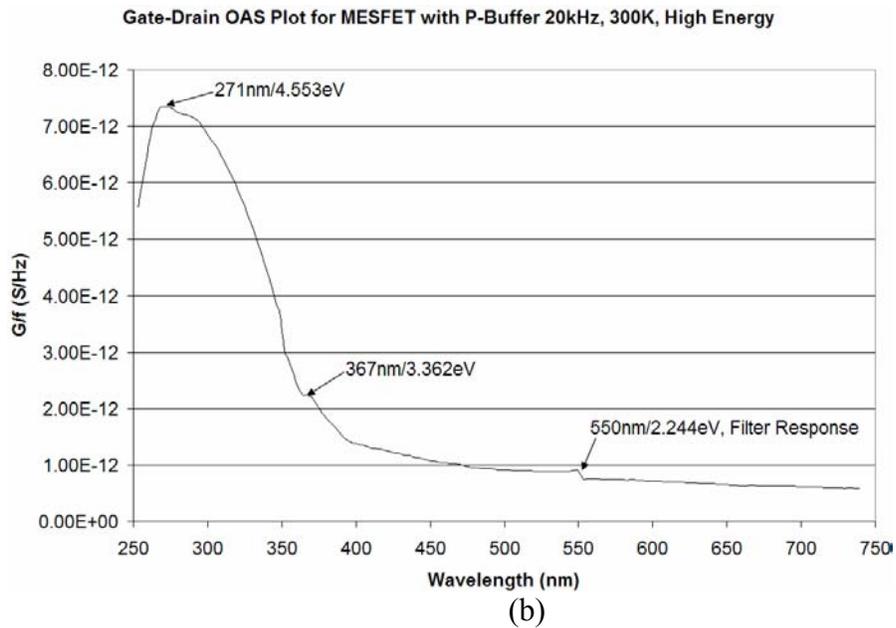
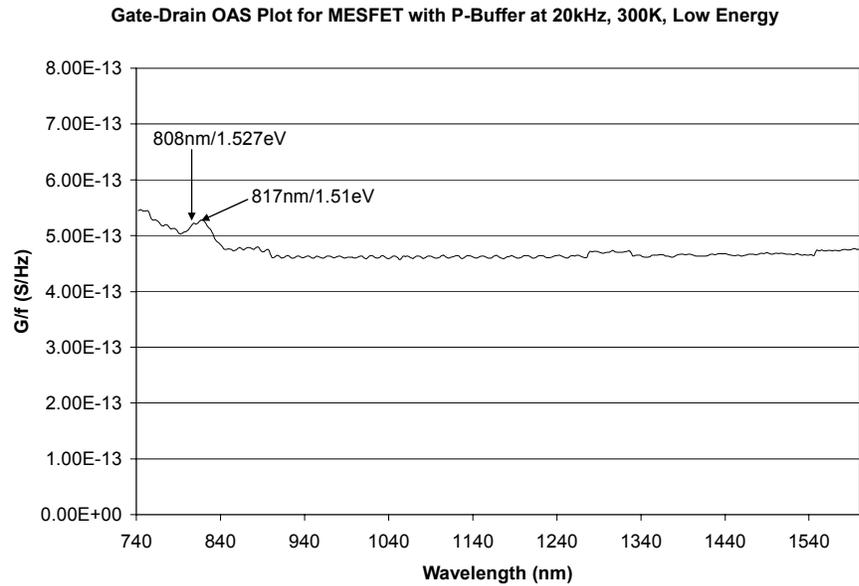
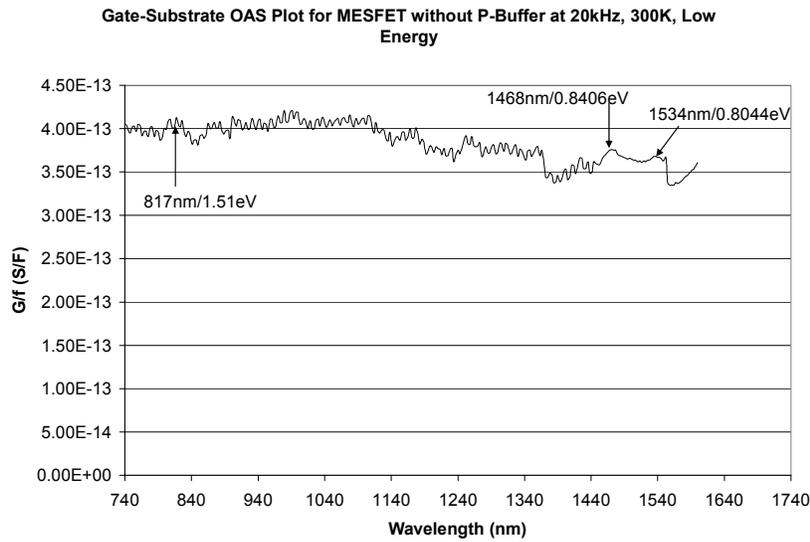
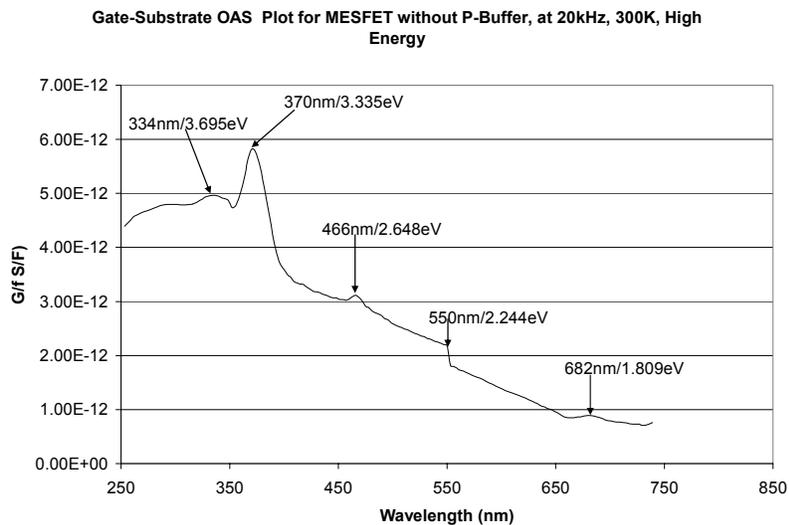


Figure 5.4: Gate-drain OAS spectrum for experimental MESFET with p-buffer at 300 K for (a) long optical wavelength (b) short wavelength. Note: the gate-source spectra are similar.

In Figures 5.5 (a) and (b), the gate-substrate OAS spectra at 300 K for the device without p-buffer for low and high optical exposure energies are shown respectively and Figures 5.6 (a) and (b) depict the corresponding spectra for the device with p-buffer layer. It can be seen that Figure 5.5b is similar to the Figure 5.3b, which shows the high-energy



(a)



(b)

Figure 5.5: Gate-substrate OAS spectrum for experimental MESFET without p-buffer at 300 K for (a) long wavelength (b) short wavelength.

gate-source OAS spectrum for the device without p-buffer, indicating that the observed peaks are substrate related. It can also be seen that Figure 5.6(b) is also similar to Figure 5.4(b), the high-energy gate-source OAS spectrum for the device with p-buffer. Just as in Figure 5.4b, the band gap peak centered at about 370nm with energy level  $E_C - 3.335$  eV has almost vanished and the peak centered at about 466nm with activation energy of  $E_C - 2.648$  eV has completely disappeared in Figure 6.6(b), further suggesting that the peaks are due to substrate traps and that the p-buffer layer is effective in isolating the channel from the substrate. It can also be seen in Figures 5.5(b) and 5.6(b) that the peak attributed to the vanadium donor at a wavelength of 682 nm with corresponding activation energy of  $E_C - 1.809$  eV has virtually disappeared in spectrum of the device with buffer in Figure 5.6(b). The fact that the vanadium donor peak appears relatively small in the spectrum of the device without buffer could be due to its relatively low concentration. The low energy gate-substrate spectrum in Figure 5.5(a) for the device without p-buffer layer does not show much discernable peaks except at wavelengths centered at about 1468 nm and 1534 nm with activation energies  $E_C - 0.8406$  eV and  $E_C - 0.8044$  eV respectively, and the small noisy broad peak centered at about 817nm with energy level  $E_C - 1.51$  eV. Much of the spectrum is noise and cannot be attributed to any particular set of traps. Similarly, the low energy gate-substrate spectrum for the device with p-buffer layer in Figure 5.6(a) shows mostly noise signals except the peak centered at a wavelength of about 817nm with energy level of  $E_C - 1.51$  eV, which also occurs in the spectrum of the device without buffer in Figure 5.5(a). It can be seen that the peaks at 1468 nm and 1534 nm in the spectrum of the device without p-buffer (Figures 5.5(a)) are

absent in the spectrum of the device with p-buffer layer (Figures 5.6(a)), suggesting that the peaks are substrate related and indicates the effectiveness of the p-buffer layer.

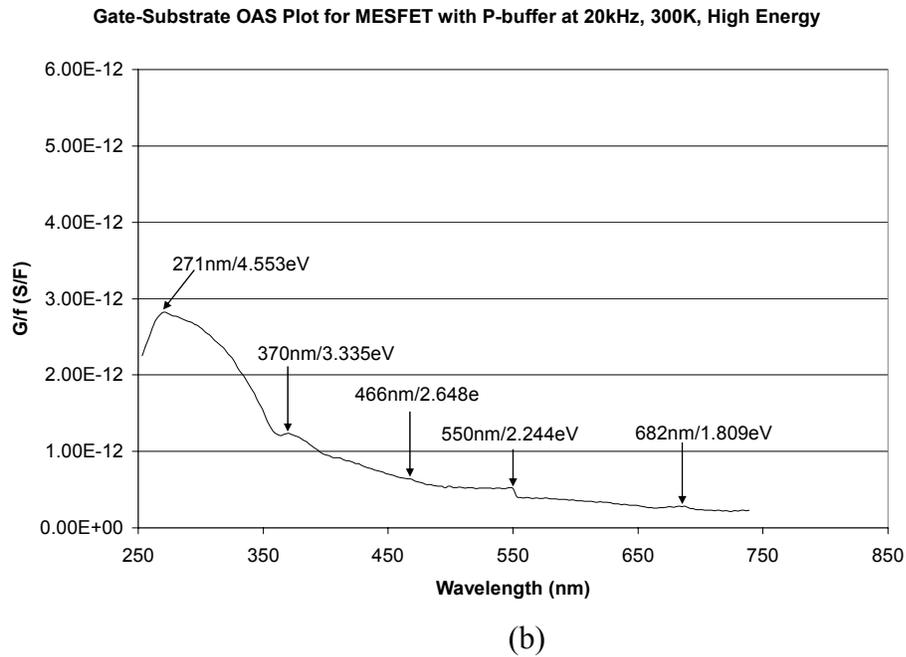
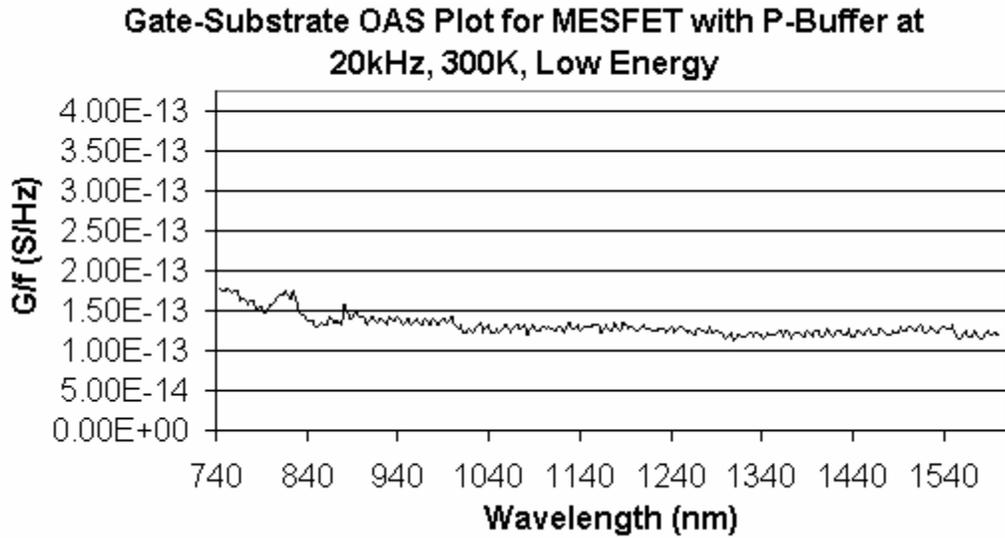


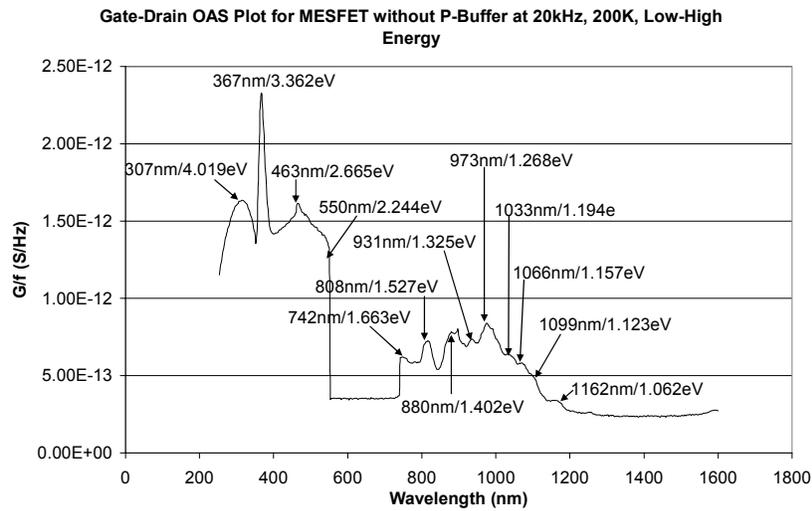
Figure 5.6: Gate-substrate OAS spectrum for experimental MESFET with p-buffer at 300 K for (a) long optical wavelength (b) short optical wavelength.

### 5.3 Results of Low Temperature (200 K) OAS Measurements

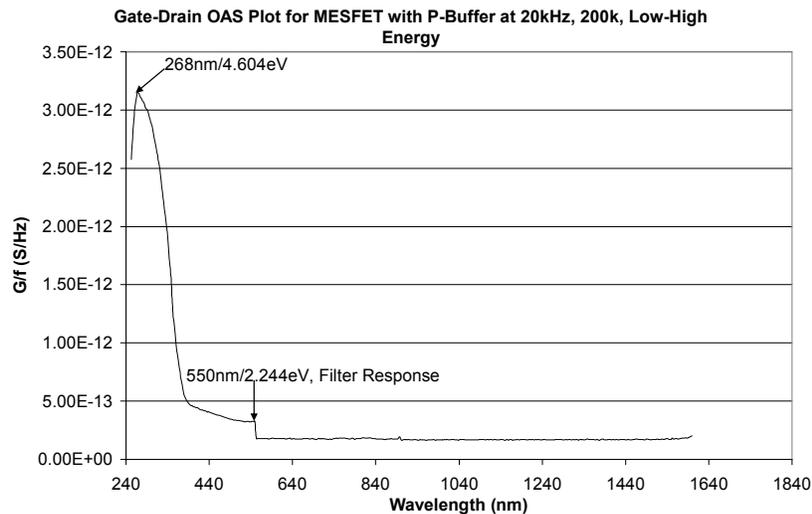
Figures 5.7(a) and 5.7(b) illustrate the low temperature full spectrum (low – high energy) gate-drain OAS plots for the device without p-buffer layer and the device with p-buffer layer respectively at 200 K. It can be observed that the peaks visible in the spectrum of the device without p-buffer layer are not resolved in the spectrum of the device with p-buffer layer with the exception of the filter response at 550 nm, which is not attributable to traps. Figures 5.8(a) and 5.8(b) show the expanded views of the gate-drain OAS spectra at low energy and high energy respectively for the device with buffer and Figures 5.9(a) and 5.9(b) depict corresponding spectra for the device without buffer. Comparing Figure 5.8(a) and Figure 5.9(a) it is observed in Figure 5.9(a) that the peak at 817 nm with activation energy of  $E_C - 1.51$  eV, which is observed in all the low energy spectra for both the devices with and without p-buffer layer at 300 K, also appears in Figure 5.8(a), the low energy spectrum for the device with buffer although it is reduced as already noted above. It has already been indicated in section 5.2 and elsewhere in this work that these peaks could be due to traps generated by source/drain residual implant lattice damage. These traps could be responsible for or at least contribute to the hysteresis observed in the drain I-V curves of the experimental devices with buffer and those without buffer, particularly at high temperatures such as 480 K.

The peak in Figure 5.9(b) at 880 nm with energy level of  $E_C - 1.402$  eV, which corresponds to the peak in Figure 5.8(a) at 874 nm with activation energy of  $E_C - 1.412$  eV appears reduced in the latter figure. It is quite plausible that the traps responsible for these peaks could also be source/drain residual implant lattice damage related and could

be related to the peaks centered at 817 nm with energy level of  $E_C - 1.51$  eV due to the close proximity of the two set of peaks. It can be argued that these two set of peaks are now resolved due to the low measurement temperature.

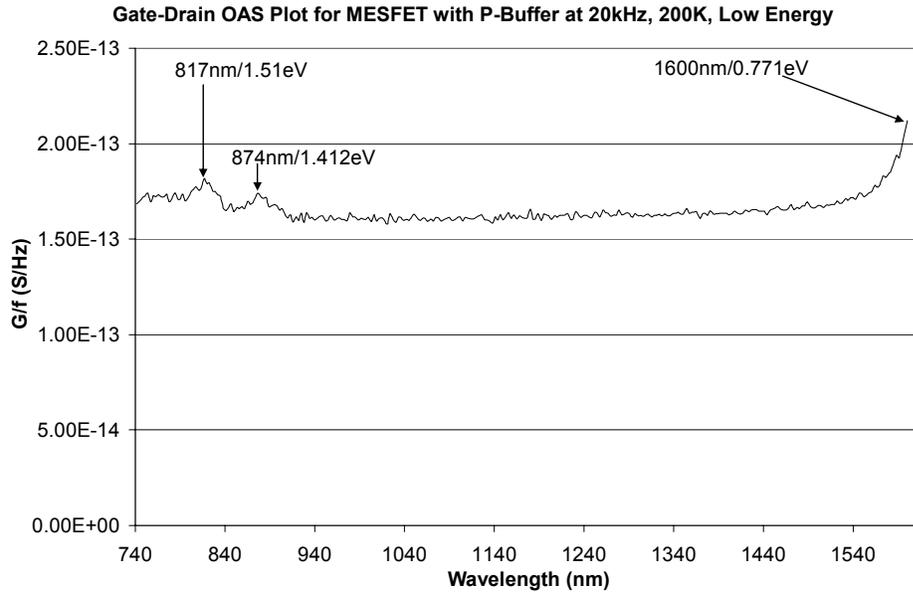


(a)

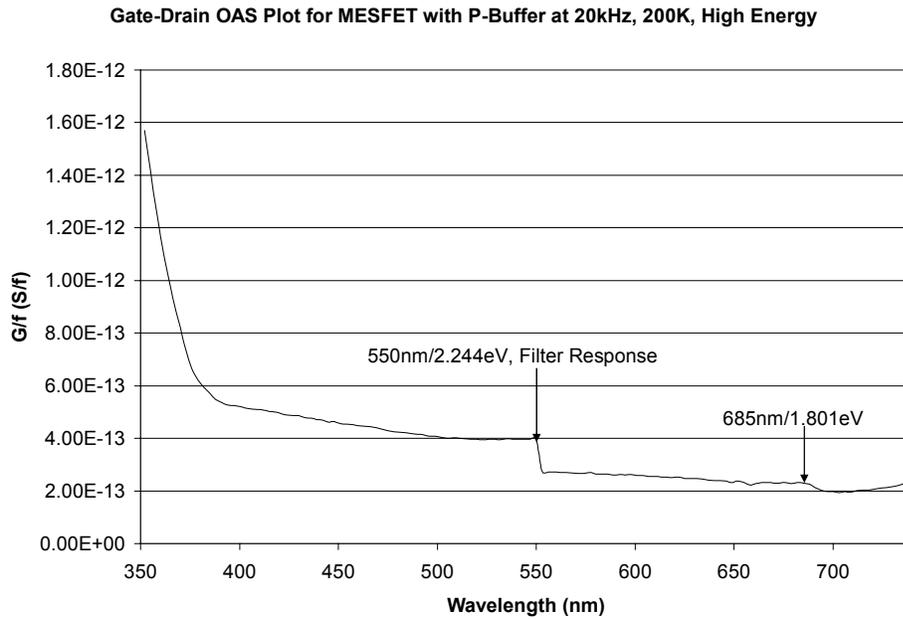


(b)

Figure 5.7: Full spectrum gate-drain OAS plot for MESFET (a) without p-buffer layer (b) with p-buffer layer, at 200 K. The gate-source spectrum is similar.



(a)



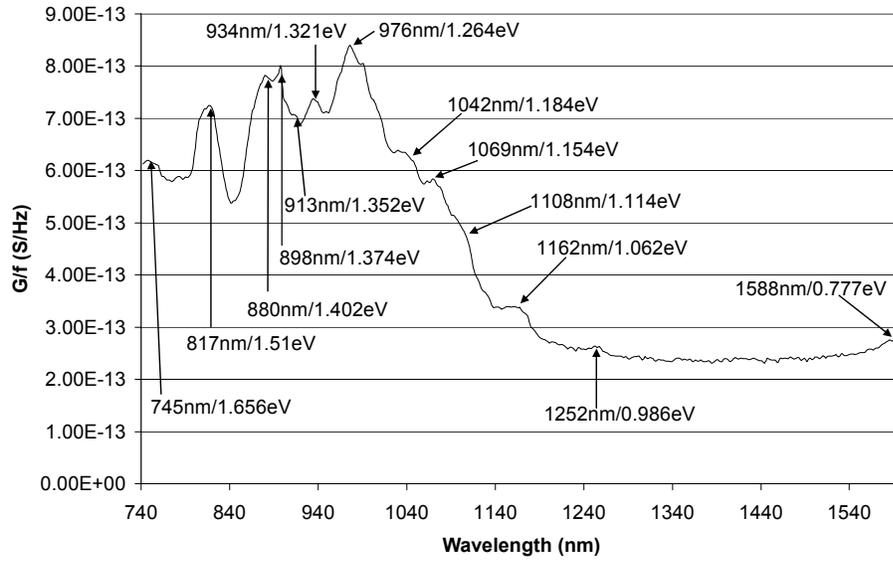
(b)

Figure 5.8: Gate-Drain OAS spectrum for experimental MESFET with p-buffer at 200 K for (a) long wavelength (b) short wavelength.

The peak at 1588 nm with activation energy of 0.777 eV in Figure 5.9(a), however, appears to about the same degree in Figure 5.8(a) at 1600 nm with energy level  $E_C - 0.771$  eV.

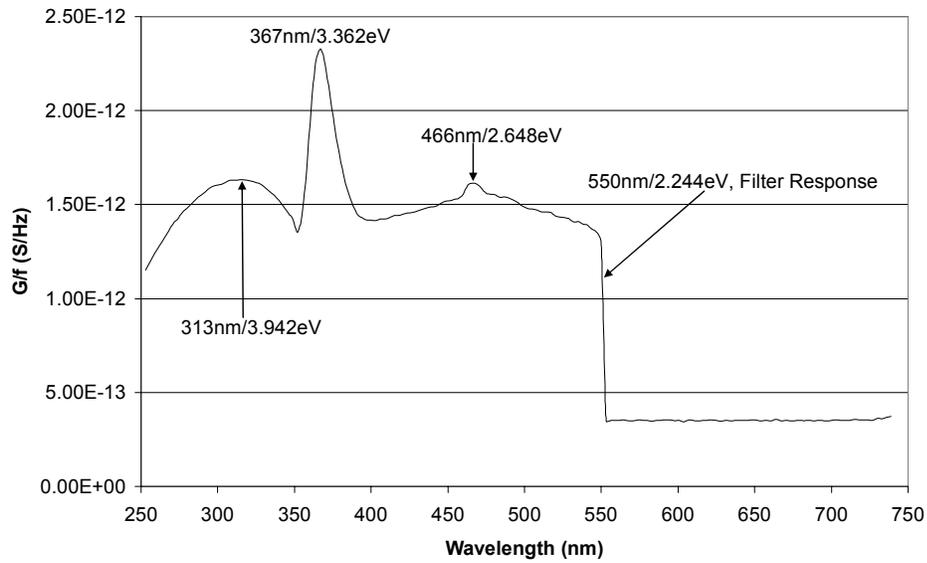
The rest of the peak in the low energy spectrum of the device without buffer in Figure 5.9(a) disappears in the spectrum of the device with buffer in Figure 5.8(a), indicating that the peaks in Figure 5.9(a) are due to substrate traps and that the p-buffer layer is effective in isolating the channel from the substrate. In the high-energy spectrum in Figure 5.9(b), the band gap peak at 347 nm with energy level of  $E_C - 3.362$  eV is prominently shown in addition to the peak at 466nm with activation of  $E_C - 2.648$  eV, which also occurs in all the high-energy spectra for the device without p-buffer layer at 300 K. However, these peaks do not appear in the high energy spectrum of the device with p-buffer in Figure 5.8(b), further suggesting that the traps responsible for the peaks in the spectrum of the device without buffer are substrate related.

Gate-Drain OAS Plot for MESFET without Buffer at 20kHz, 200K, Low Energy



(a)

Gate-Drain OAS Plot for MESFET at 20kHz, 200K, High Energy



(b)

Figure 5.9: Gate-Drain OAS spectrum for experimental MESFET without p-buffer at 200 K for (a) long optical wavelength (b) short optical wavelength.

Figure 5.10(a) shows the low energy gate-source spectrum at 200 K for the device with p-buffer layer and Figure 5.10(b) shows the corresponding high-energy spectrum. Figures 5.11 (a) and (b) illustrate, respectively the low energy and high energy gate-source spectra for the device without buffer. As can be seen much of the low energy spectrum in Figure 5.10(a) is made up of noise signals, which cannot be attributed to any defect traps as it has already been observed above. The peak centered at 814 nm with activation energy of  $E_C - 1.516$  eV in Figure 5.10(a) corresponds to the peak centered at 811 nm with energy level  $E_C - 1.521$  eV in the spectrum of the device without buffer in Figure 5.11(a). These two peaks correspond to the peak centered at 817 nm with energy level  $E_C - 1.51$  eV, which has been observed in the low energy spectra of both types of devices at 300 K. As already indicated above, these peaks could be attributed to source/drain residual implant lattice damage traps, since traps with similar activation energies in the range of ( $E_C - 1.49$  eV) and ( $E_C - 1.60$  eV) have been observed by T. Dalibor et al. [8] after  $He^+$ -implantation of n-type 4H-SiC CVD Epilayers. It can be seen in Figure 5.10(a) that the 814 nm peak appears in addition to filter response at about 900 nm, which is not related to defect traps. It can also be seen in the low energy gate-source spectrum of the device without buffer in Figure 5.11(a) that except for the peak at 811 nm, the remaining peaks do not appear in the spectrum of the device with buffer in Figure 5.10(a).

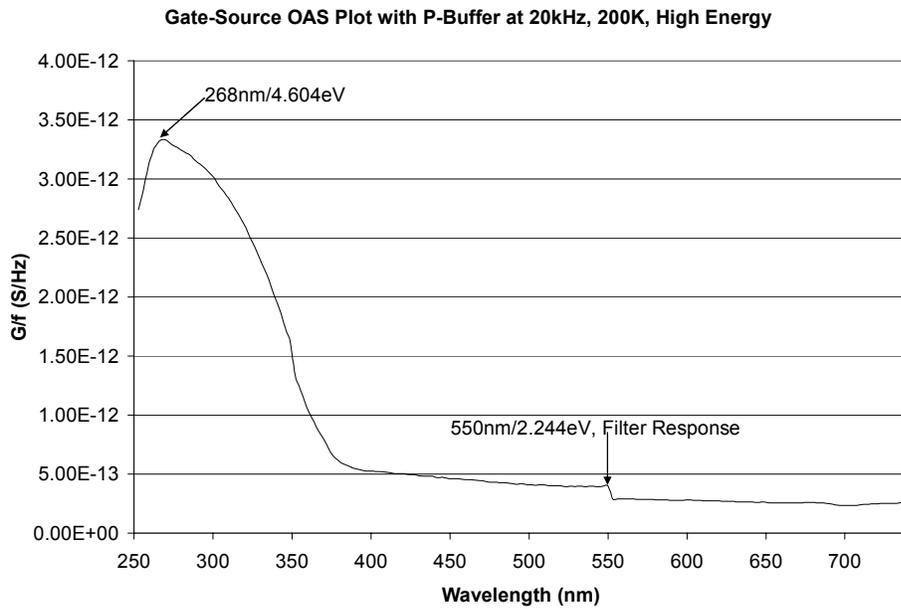
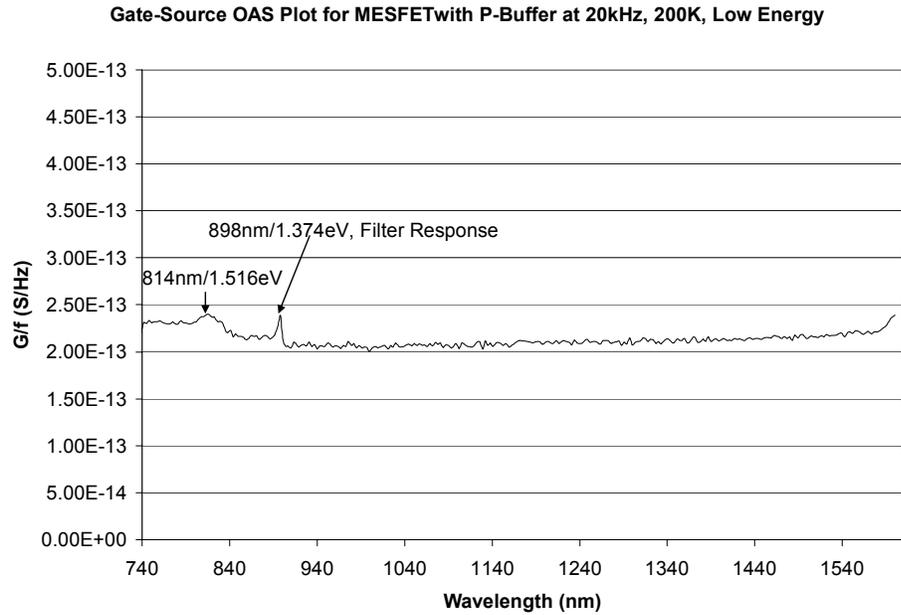
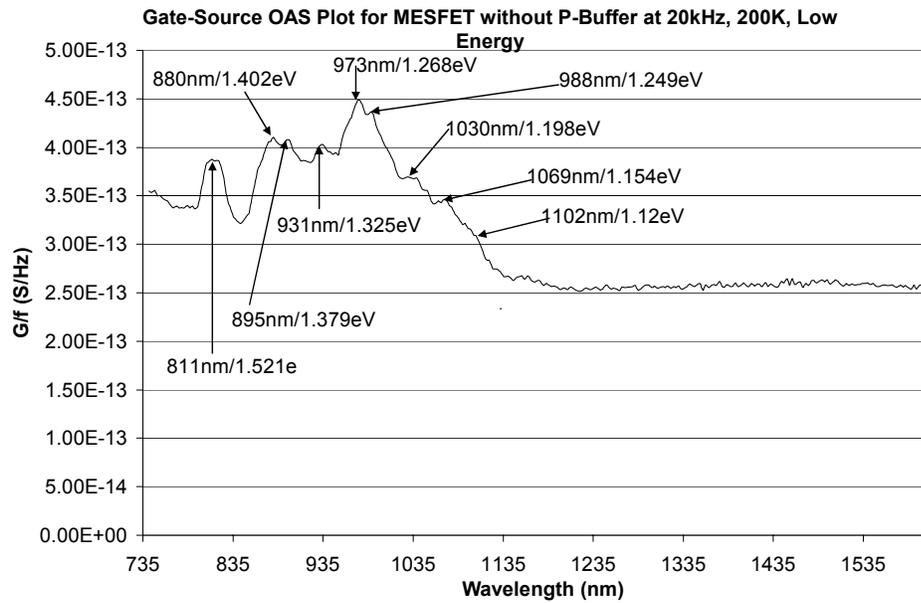
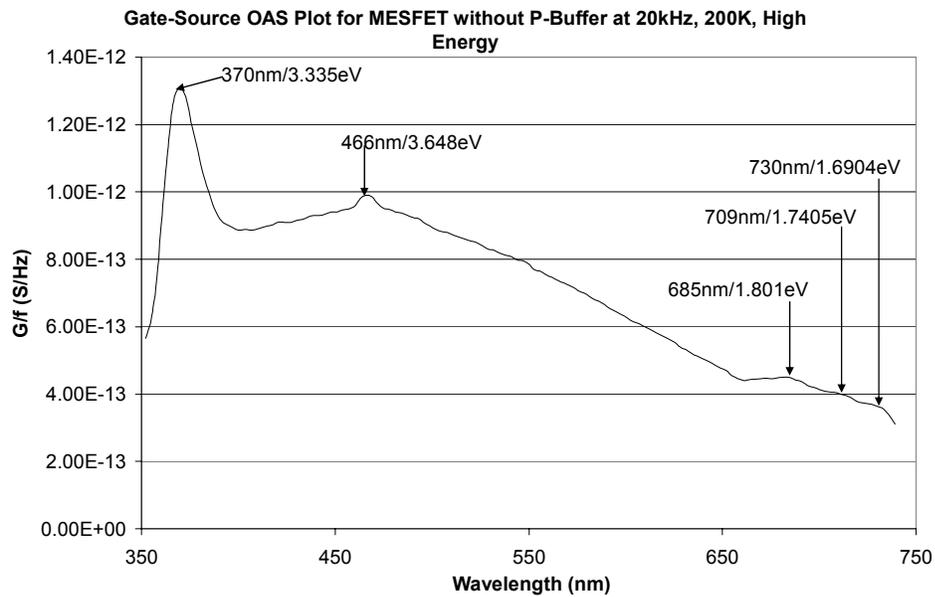


Figure 5.10: Gate-source OAS spectrum for experimental MESFET with p-buffer at 200 K for (a) long optical wavelength (b) short optical wavelength.



(a)



(b)

Figure 5.11: Gate-source OAS spectrum for experimental MESFET without p-buffer at 200 K for (a) long optical wavelength (b) short optical wavelength.

Comparing the high-energy spectrum in Figure 5.11(b) for the device without p-buffer to that for the device with p-buffer in Figure 5.10(b), it can be observed again that the band gap peak at 370 nm and the rest of the peaks in Figure 5.11(b) are non-existent in Figure 5.10(b).

## CHAPTER VI

### DISCUSSIONS AND CONCLUSIONS

As it has already been stated in Chapter III of this report, DC characterization of 4H-SiC power MESFETs with and without p-buffer layers showed hysteresis in the drain I-V characteristics of both types of devices to about the same degree at 300 K and at 480 K, which is attributed to traps due to crystal defects, although the hysteresis in the drain I-V curves at 480 K is reduced relative to that at 300 K, as shown in Figures 3.1 and 3.2. This is due to thermal emission of electrons from trap levels at high temperatures into the conduction band, where they become available for conduction. However, thermal gate-source and output (drain-source) spectroscopic measurements on the two types of devices could detect traps only in the MESFETs without the p-buffer layer, as illustrated in Figure 3.3. The traps observed in the thermal spectroscopic measurements have energy levels that vary between  $E_C - 0.95$  eV and  $E_C - 1.06$  eV, as shown in Figure 3.4, and are consistent with vanadium acceptors in the substrate.

Device simulations (Chapter IV) using the two-dimensional device simulator, Medici™, also showed hysteresis in the drain I-V characteristics of both types of devices at 300 K and 480 K, as shown in Figures 4.3 and 4.4. Further simulations showed that in addition to deep SI substrate traps, which are known to be a major source of hysteresis in the drain I-V characteristics of MESFET, source/drain residual implant lattice damage traps could also contribute to the hysteresis at 300 K and are solely responsible for the

hysteresis at 480 K, as illustrated in Figures 4.7(a) and (b). Simulations show that the hysteresis due to SI substrate traps disappears at high temperatures such as 480 K (Figure 4.5(b) and Figure 4.6(b)). However, the hysteresis in the drain I-V curves of MESFETs with traps simulating only source/drain residual implant lattice damage persists at 480 K albeit reduced relative to that at 300 K. The reduction in the degree of hysteresis at high temperatures is due to thermal emission of electrons from the trap levels, as already indicated above and in Appendix A. In all the simulations, the hysteresis in the drain I-V curves at high temperatures such as 480 K are reduced compared to that at 300 K, as observed in the experimental drain I-V curves. It is only the hysteresis in the simulated drain I-V curves of MESFETs with semi-insulating substrate traps that vanish at high temperatures such as 480 K. The above observations suggest that the hysteresis that persists at 480 K in the experimental devices could be attributed solely to the source/drain residual implant lattice damage traps.

As already inferred in Chapter IV, device simulations show that the hysteresis in the drain I-V curves of a MESFET with traps simulating only source/drain residual implant lattice damage decreases with increasing negative  $V_{GS}$  bias. Comparing Figure 3.2, which is a typical drain I-V characteristics of both the experimental devices with p-buffer layer and those without p-buffer at 480 K, and Figure 4.7, which is the simulated drain I-V curves of a MESFET on p-type substrate with traps representing only source/drain implant damage traps at 300 K and 480 K, it can be seen that the hysteresis decreases as  $V_{GS}$  in both figures. This observation further leads to the inference that the hysteresis in the drain I-V characteristics of the experimental devices at 480 K could be

attributed solely to source/drain residual implant lattice damage traps. Comparing Figures 3.1 and 3.2, which represent typical drain I-V curves of both types of experimental devices at 300 K and 480 K respectively, it can be seen that the large hysteresis lobe at  $V_{GS} = -20$  V in Figure 3.1 is drastically reduced in Figure 3.2, the I-V characteristics at 480 K. As exhibited in Chapter IV, hysteresis in the simulated drain I-V characteristics of a MESFET with only semi-insulating substrate traps increase with decreasing  $V_{GS}$ , as shown in Figure 4.5(a) and Figure 4.6(a), and the hysteresis disappears at high temperatures such as 480 K as shown in Figure 4.5(b) and Figure 4.6(b). It can therefore be inferred that at 300 K, much of the hysteresis in the drain I-V characteristics of the experimental MESFETs at large negative  $V_{GS}$ , such as  $V_{GS} = -20$  V and beyond, could be attributed to semi-insulating substrate traps and much of the hysteresis at small negative  $V_{GS}$  could be attributed to source/drain residual implant lattice damage traps. It has already been inferred above that all the hysteresis in experimental drain I-V curves of the devices at 480 K are due to source/drain residual implant lattice damage traps, since simulations show that it is only the hysteresis due to these traps that remain at 480 K.

Further simulation results in Chapter IV show that the hysteresis due to traps representing source/drain residual implant lattice damage traps is attributable to the volume of traps within the lateral straggle of implanted the source and drain regions at right side of the source and the left side of the drain in the channel region, as illustrated in Figures 4.8 – 4.14 and discussed in Appendices A and B. If the traps within the lateral straggle regions are removed the hysteresis in the drain I-V curves disappears. As explained in Chapter IV, this is because the current flows mainly between the inside

edges of the source and drain through the lateral straggle regions, as illustrated in Figures 4.15 – 4.17.

Simulations further suggest that if the channel traps are uniformly distributed spatially within the channel, the hysteresis in the drain I-V curves increases with increasing negative  $V_{GS}$ , just as it occurs in the I-V curves of MESFETs with only SI substrate traps and discussed in Chapter IV and Appendix A. As shown in Chapter IV and Appendix A, it is only when the channel traps are restricted to the lateral straggle regions of the source and drain that the hysteresis in the simulated drain I-V curves decreases with increasing negative  $V_{GS}$ , as it occurs in the drain I-V curves of the experimental devices, particularly at 480 K. It could therefore be inferred that the hysteresis in the drain I-V characteristics of the experimental could largely be attributed to source/drain residual implant lattice damage traps localized in the lateral straggle regions of the source and drain, particularly at 480 K.

As already reviewed in Chapter I, section 1.3, it well established in the literature that ion implantation and any high-energy particle bombardment of semiconductors cause crystal lattice damage, which generate traps with energy levels distributed within the semiconductor band gap. However, all previous investigations into hysteresis in the drain I-V characteristics of MESFETs have been attributed to semi-insulating substrate traps. The possibility that traps due to residual implant lattice damage could at least contribute to hysteresis in the drain I-V curves of MESFETs and other implanted devices has been ignored in the literature, as already observed elsewhere in this report. In this dissertation it has been shown that residual implant lattice damage traps could at least contribute to

hysteresis in drain I-V curves of MESFETs and other implanted devices, if not solely responsible.

Since the activation energies of the traps detected by thermal spectroscopic measurements in the devices without buffer are consistent with semi-insulating substrate traps due to vanadium acceptors it is quite plausible the traps responsible for the hysteresis in the drain I-V curves of both types of experimental MESFETs could be due to source/drain residual implant lattice damage traps as suggested by device simulation. The implant damage traps could at least contribute to the hysteresis. Furthermore, it is plausible that the energy levels of these source/drain implant damage traps could be too deep in the 4H-SiC band gap to be detected by thermal spectroscopic measurements. This is because high temperatures may have to be used to thermally excite carriers from the trap levels in order to detect the traps. These high measurement temperatures could damage the devices and therefore optical admittance spectroscopy (OAS) was used to aid in the detection of the implant damage traps, which this thesis concludes are largely responsible for the hysteresis at 300 K and solely responsible for the hysteresis at 480 K.

It is evident from Chapter V that the OAS measurements performed on both the devices with and without p-buffer layer showed several peaks in the OAS spectra of the device without p-buffer, which are absent or reduced in the spectra of the device with p-buffer. These observations indicate that the traps responsible for the peaks in the OAS spectra of the devices are largely substrate related and that the p-buffer layer is effective in isolating the channel from the substrate. As it has already been observed in Chapter V, an OAS peak with optical wavelength centered between 808 nm and 818 nm with

corresponding trap energy level between ( $E_C - 1.527$  eV) and ( $E_C - 1.508$  eV) appears in the OAS spectra of both the device with p-buffer layer and the device without buffer, although the peak in the spectra of the device with buffer is reduced. A similar peak with activation energy between ( $E_C - 1.49$  eV) and ( $E_C - 1.60$  eV) has been observed by T. Dalibor et al. [8] in the DLTS spectrum of n-type 4H-SiC CVD epilayers after He<sup>+</sup>-implantation and anneal, as illustrated in Chapter I. The authors attribute the observed peak to intrinsic defects traps generated by lattice damage as a result of the ion bombardment of the SiC crystal lattice. Since traps detected are intrinsic in nature, it can be argued that they can be generated by any high-energy particle bombardment of the 4H-SiC crystal lattice. Hence the traps, centered between 808nm and 818nm with corresponding activation energy between ( $E_C - 1.527$  eV) and ( $E_C - 1.508$  eV), observed in the OAS spectra of the experimental MESFETs can be generated by the N<sup>+</sup>-implantation doping of nitrogen into the n-type CVD epitaxial channel, which was used to form the source and drain ohmic contact regions. The broad nature of the 808 nm – 818 nm peak suggests that the traps responsible for this peak could have distributed energy levels in the 4H-SiC bandgap. As pointed out in Chapters IV and V, this is consistent with traps due to residual implant lattice damage, since implant damage generally results in several traps with energy levels distributed in the semiconductor bandgap.

The fact that the peak in the OAS spectrum of the MESFET with buffer is reduced relative to the peak in the spectrum of the device without buffer can be explained by the realization that implant damage can extend beyond the projected range, as

observed by Koshka et al. [13]. As such, it is quite plausible that the implant damage in both types of experimental MESFETs extends beyond the source and drain ohmic contact depths of 0.2  $\mu\text{m}$  and into the substrate or p-buffer and that the p-buffer layer is effective in screening the buffer portion of the implant damage traps in the device with buffer. It must be noted that the implant lattice damage may not make it past the buffer into the substrate in devices with buffer. Here, it should also be noted that the p-buffer layer has already been shown in Chapter V to be effective in isolating the channel from the substrate. This could explain why the peaks, centered between 808 nm and 818 nm in the spectra of the device with buffer is reduced compared with the corresponding peaks in the spectra of the device without the p-buffer layer. Thus the 808 nm – 817 nm peak that appears in the spectra of the device with buffer is consistent with the assertion that the channel contains implant damage traps of the type that simulations show, produce the observed hysteresis. In contrast, the 808 nm – 818 nm peak that appears in the spectra of the device without buffer could be due to both the substrate and channel portions of the implant damage traps.

Since the hysteresis in the drain I-V characteristics of both the experimental MESFET with buffer and the MESFET without buffer occur to about the same magnitude, it could not be due largely to substrate traps. If that were the case, then the hysteresis would be more pronounced in the I-V curves of the device without p-buffer than in the I-V curves of the device with buffer. Now, it has been shown in the OAS spectra of both types of devices in Chapter V that the p-type buffer layer is effective in screening the channel from the substrate. Therefore the hysteresis in the drain I-V

characteristics of both types of devices is probably due mostly to similar traps with similar parameters and concentrations. The OAS spectra in Chapter V shows that it is only the peaks centered around 817 nm with activation energy of about ( $E_C - 1.51$  eV) that appear consistently in the OAS spectra of both types of devices. Since the hysteresis in the I-V curves of both types of devices occur to about the same degree, then it is quite plausible, and the simulations presented here bear this out, that the hysteresis could be attributed largely to the channel portion of the source/drain residual implant damage traps, particularly at 480 K.

It is legitimate and necessary to be concerned about hysteresis in the I-V curves of devices because hysteresis in device I-V curves is a manifestation of the presence of traps due to defects somewhere in the device. These traps trap and emit carriers over time. The trapping and emission of carriers are scattering processes, which lead to reduced carrier mobility, which in turn limits high speed and high frequency device operations. Carrier trappings also lead to reduced carrier concentration and hence reduced current levels depending on how long the carriers remain trapped. Reduction in the current levels in the final analysis leads to reduction in device power levels. Furthermore, trapping and emission of carriers could also lead to the generation of device noise, since trapping and emission of carriers are random processes. Thus the presence of traps in devices reduces the overall device performance and has to be addressed and rectified. Furthermore, in a fully implanted MESFET in which the source/drain ohmic contact regions and channel are all implanted, the presence of residual implant lattice damage traps should be of great concern and should be addressed.

In conclusion, considering all the observations and inferences drawn above and in the preceding chapters, the most plausible explanation at this time is that the hysteresis observed in the experimental drain I-V characteristics of the MESFETs with and without p-buffer layer at 300 K is due largely to source/drain residual implant lattice damage traps resulting from the lateral straggle. Furthermore, it has been shown here that the source/drain residual implant damage traps are solely responsible for the hysteresis that occurs in the I-V curves of the MESFETs at 480 K. In addition the hysteresis in the experimental device I-V curves at large negative  $V_{GS}$  at 300 K could be attributed partly to SI substrate traps, while the hysteresis at small negative  $V_{GS}$  at 300 K could largely be attributed to source/drain residual implant lattice damage traps.

## 6.1 Future Work

Due to equipment limitations the highest optical wavelength that could be used to probe the experimental devices in the OAS measurements was about 1600 nm, which is equivalent to an energy level of about  $E_C - 0.77$  eV. Thus the OAS measurements could probe the 4H-SiC bandgap from the top valence band,  $E_V$ , to an energy level of about 0.77 eV below the edge of the conduction band,  $E_C$ . As further work, the optical wavelength will be extended so that the entire 4H-SiC bandgap can be probed to reveal any traps with energy levels between  $E_C - 0.77$  eV and  $E_C$  that might be present. In addition work will be performed to locate the actual spatial location of the residual implant lattice damage traps in the channel to further validate their presence. Surface traps will also be simulated to investigate their effect on device I-V curves.

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## APPENDIX A

### PHYSICS OF HYSTERESIS – SIMULATION APPROACH

## APPENDIX A

### Physics of Hysteresis – Simulation Approach

The hysteresis (looping) in the drain I-V characteristics of MESFETs is due to the capture (trapping) and emission (detrapping) processes of deep level traps in the substrate and/or the channel and surface of the devices. When the period (pulse width) of the drain voltage is close to the time constant of the trapping process, a steady-state trap occupation or ionized (donors devoid of electrons and acceptors filled with electrons) trap distribution cannot be reached during the drain voltage swing [16]. As  $V_{DS}$  rises from 0V to  $V_{DS(max)}$  and falls back to 0V electron capture will dominate at certain portions of the drain voltage swing and electron emission will dominate at the other portions [16].

#### A.1 MESFET with Substrate Traps only – no p-Buffer Layer

Figure A.1 shows the simulated drain I-V characteristics at  $V_{GS} = -20$  V for a 0.5  $\mu\text{m}$  4H-SiC MESFET with SI substrate acceptor traps only and no p-buffer layer, and Figure A.2a shows the simulated plots of the conduction band edge under the gate (along the center of the gate) for various drain-source voltages ( $V_{DS}$ ) and corresponding times at  $V_{GS} = -20$  V and  $T = 300$  K. Figure A.2b shows an expanded view of the plots. The hysteresis (looping) in the drain I-V characteristics of MESFETs is due to the presence of electron traps on the substrate side of the channel-substrate, which trap channel electrons [16,17,18]. The electron traps can be either deep neutral acceptors or ionized donors

when they are empty depending on the compensation mechanism used to achieve the semi-insulating characteristics of the substrate [14, 16]. In our present case, the deep level traps are neutral acceptors (empty acceptors) with energy level of 0.63 eV above mid-gap, which become negatively charged when occupied by electrons. So when the deep level acceptors on the substrate side of the channel-substrate interface trap channel electrons, a negative space charge (due to the trapped electrons) is set up on the substrate side of the interface. This negative space charge sets up (induces) a symmetric depleted positive space charge region on the lower part of the channel [14], constricting the channel and hence reducing the drain current. The width of the negative space charge region on the substrate side of the channel-substrate interface due to the trapped electrons is modulated by the drain-source voltage ( $V_{DS}$ ), as it rises and falls depending on how much electrons are trapped. As such, the width of the corresponding symmetric space charge region on the lower portion of the channel is also modulated by  $V_{DS}$  as it rises and falls, leading to the hysteresis in the drain I-V characteristics. The negative space charge on the substrate side of the channel-substrate interface therefore acts as parasitic gate, which results in drain current decrease or collapse [14, 16]. The parasitic gate is referred to as backgate in the literature and its corresponding effect, the back-gating effect.

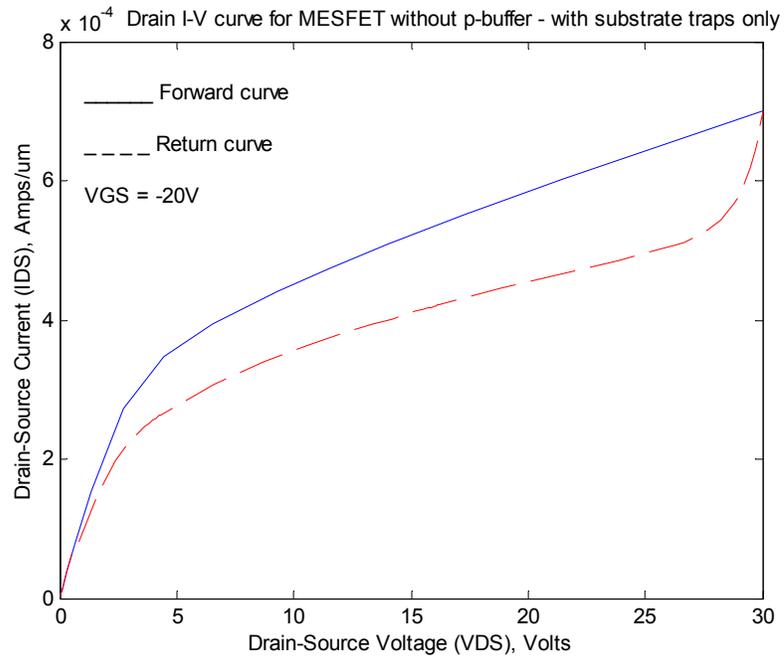
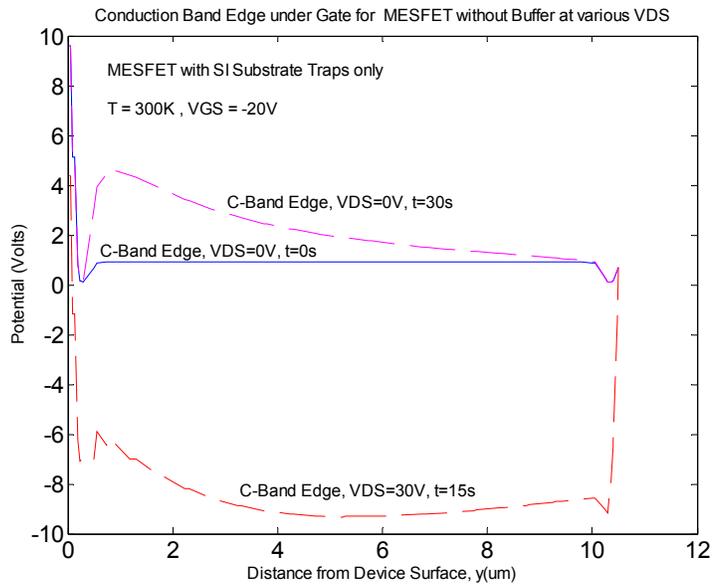
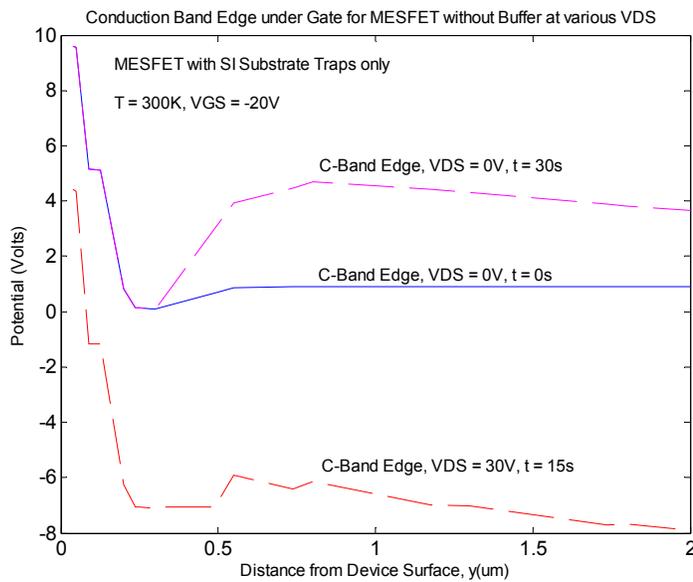


Figure A.1: Simulated drain I-V characteristics for MESFET with substrate traps only – without p-buffer layer. Note the large degree of hysteresis (looping) in the I-V curve.



(a)



(b)

Figure A.2: Conduction band edge under the gate for 0.5  $\mu\text{m}$  4H-SiC MESFET without p-buffer for various  $V_{DS}$  and times at  $V_{GS} = -20$  V for (a) entire device depth (b) an expanded view.

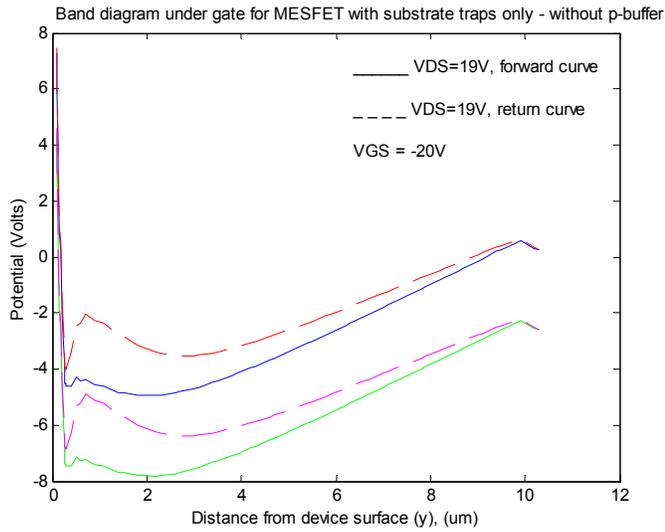
The simulation is performed with a triangular pulse of 30 V amplitude and pulse width of 30 s. Therefore it takes 30s for  $V_{DS}$  to swing from 0 V to 30 V and back to 0 V. From Figure A.2b, we see that electron capture and emission largely takes place on the substrate side of the channel-substrate interface, although some capture and emission processes also take place in the substrate, comparing the conduction band edge diagrams at  $V_{DS} = 30$  V,  $t = 15$  s and  $V_{DS} = 0$  V,  $t = 30$  s to that at  $V_{DS} = 0$  V,  $t = 0$  s. The channel-substrate interface occurs at a distance of  $y = 0.3$   $\mu\text{m}$  from the device surface, as the channel width is 0.3  $\mu\text{m}$ . At  $V_{DS} = 0$  V,  $t = 0$  s, there is an initial trapping of channel electrons leading to a potential build up (about 1 V) at the channel-substrate interface beginning from about  $y = 0.3$   $\mu\text{m}$ . Comparing the conduction band edge plot at  $V_{DS} = 0$  V,  $t = 0$  s to that at  $V_{DS} = 30$  V,  $t = 15$  s, we see that although capture and emission compete as  $V_{DS}$  rises and falls, electron emission is the dominant process as  $V_{DS}$  rises from  $V_{DS} = 0$  V,  $t = 0$  s. As a result, the onset of the potential barrier has been shifted from  $y = 0.3$   $\mu\text{m}$  at  $V_{DS} = 0$  V,  $t = 0$  s to  $y = 0.5$   $\mu\text{m}$  at  $V_{DS} = 30$  V,  $t = 15$  s. Although the potential barrier at  $V_{DS} = 30$  V,  $t = 15$  s is also about 1 V, the shape and nature of the conduction band edge suggest that electrons have been emitted from traps at the channel-substrate interface and in the substrate, giving the shift in the onset of interface potential barrier rise and the slope in the conduction band edge potential in the substrate. Hence, because of the slope in the substrate conduction band edge, any electron injected over the barrier will quickly be drawn into the substrate and be trapped by the substrate traps. Comparing the slope in the conduction band edge potential in the substrate at  $V_{DS} = 0$  V,  $t = 0$  s to that at  $V_{DS} = 30$  V,  $t = 15$  s, we recognize that it will be easier for electrons

injected over the interface potential barrier to be drawn (attracted) into the substrate in the latter case, due to the increased potential slope, and be trapped by substrate traps than in the former case where the conduction band edge potential is virtually flat (zero slope). As such, at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$ , electron capture will begin to be the dominant process.

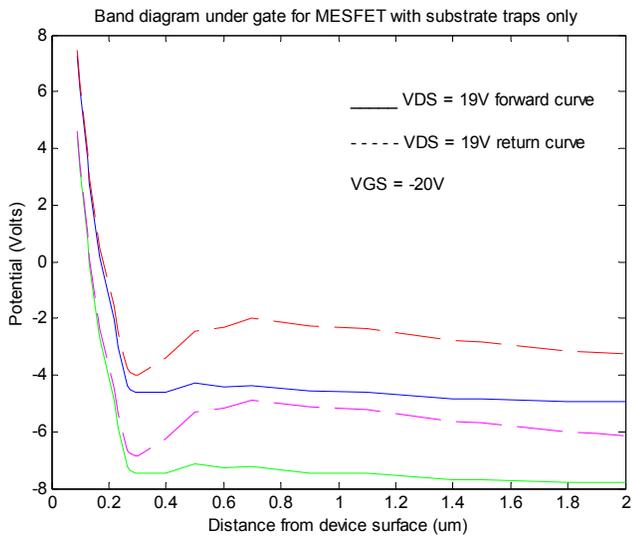
Now, comparing the conduction band edge potential at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$  to that at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ , we observe that as  $V_{DS}$  falls from  $30 \text{ V}$  back to  $0 \text{ V}$ , due to electron capture, the interface potential barrier has increased from about  $1 \text{ V}$  at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$  to about  $5 \text{ V}$  at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ . At such a high interface potential barrier, only the most energetic electrons will have enough energy to overcome the barrier and be drawn into the substrate and get trapped by substrate traps. As a result, at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ , electron emission will be the dominant process. From the above treatment we realize that, at  $V_{DS} = 0 \text{ V}$  electron emission is the dominant process and at  $V_{DS} = V_{DS} (\text{max}) = 30 \text{ V}$  electron capture is the dominant process. Hence, as  $V_{DS}$  rises from  $0 \text{ V}$  to  $V_{DS} (\text{max})$  the electron emission dominant process gradually gives way to an electron capture dominant process, and as  $V_{DS}$  falls from  $V_{DS} (\text{max})$  to  $0 \text{ V}$ , the electron capture dominant process gradually gives way to an electron emission dominant process. These processes will lead to difference in trap occupation (empty, unoccupied trap distribution) and free electron concentration, and therefore the drain current as  $V_{DS}$  rises and falls at a given  $V_{GS}$  and  $V_{DS}$ , resulting in hysteresis (looping) in the drain I-V characteristics. Here, we note that it is the *difference* in trap occupation (empty trap concentration) and free electron concentration, and hence drain current as  $V_{DS}$  rises and falls, at a given  $V_{DS}$ , due to the emission and capture of free electrons by traps that lead to hysteresis (looping) in the

drain I-V characteristics. If there is no difference in the trap occupation (empty trap distribution) and free electron concentration at a given  $V_{DS}$  as  $V_{DS}$  rises and falls, there will be no difference in drain current as  $V_{DS}$  rises and falls, and therefore no hysteresis (looping) in the drain I-V characteristics, as will be shown below.

Figure A.3a shows the band diagrams under the gate (along the center of the gate) at  $V_{DS} = 19$  V for  $V_{GS} = -20$  V for the forward ( $V_{DS}$  rising) and return ( $V_{DS}$  falling) curves with  $V_{DS(max)} = 30$  V. Figure A.3b shows the expanded view of the band diagram plots. The forward band diagram shows little or no band bending (potential barrier) at the channel-substrate interface due to electron emission, hence, the channel electrons have enough energy to overcome the potential barrier height and be injected into the substrate and get trapped there. Therefore electron emission, which is the dominant process at the beginning of the  $V_{DS}$  rise at  $V_{DS} = 0$  V is gradually turning into an electron capture dominant process.



(a)



(b)

Figure A.3: Band diagram under the gate for MESFET with substrate traps only for  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  for the forward curve (solid curve) and return curve (dashed curve) for (a) entire device depth (b) an expanded view.

The band diagram for the return curve, on the other hand, shows greater band bending (higher potential barrier) at the channel-substrate interface due to electron capture. The potential barrier at the interface is formed, during the capture-dominant

phase when  $V_{DS}$  is rising and falling in the vicinity of  $V_{DS(max)} = 30$  V by the injection of free electrons from the channel into the substrate where they are trapped [16, 17], as predicted by the Poisson's equation. At thermal equilibrium, the diffusion current due to the injection of electrons into the substrate is balanced by the drift-current from the substrate, the transient response of the barrier is mainly then controlled by the deep-level traps in the substrate [17]. As electrons are captured, by substrate traps the potential barrier at the channel-substrate interface builds up. In Figure A.3b we see that, the interface potential barrier on the return curve at  $V_{DS} = 19$  V has increased to about 2 V from about 1 V at  $V_{DS(max)} = 30$  V due to electron capture. The interface potential barrier will continue to increase as electrons continue to be captured as  $V_{DS}$  falls to 0 V until it reaches its maximum value of about 5 V at  $V_{DS} = 0$  V as shown in Figure A.2b (the  $V_{DS} = 0$  V,  $t = 30$  s curve). We note that at  $V_{DS} = 0$  V,  $t = 30$  s the high interface potential barrier of 5 V suggests that electron emission is the dominant process as already pointed out above. Thus the electron capture dominant process around  $V_{DS(max)} = 30$  V has gradually changed to an electron emission dominant process around  $V_{DS} = 0$  V. As we have already stated, the emission of electrons from trap centers as  $V_{DS}$  rises from 0 V and the capture of electrons by trap centers as  $V_{DS}$  falls from 30 V lead to difference in trap occupation and free electron concentration as  $V_{DS}$  rises and falls as shown in Figure A.3 and Figure A.4 below. This in turn leads to difference in drain current as  $V_{DS}$  rises and falls, leading to hysteresis in drain characteristics.

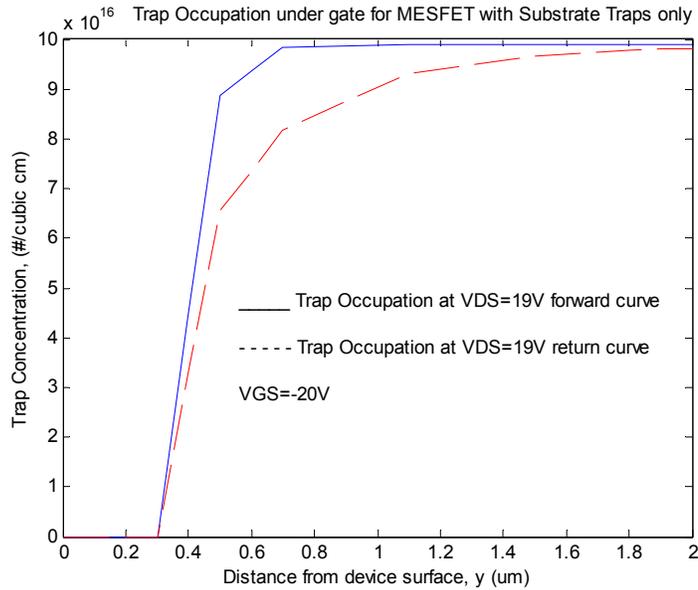


Figure A.4: Empty (unoccupied) trap distribution under the gate for MESFET with only substrate traps for  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  for the forward curve (solid curve) and return curve (dashed curve). Note that the figure actually shows the density of empty, unoccupied electron traps (acceptors).

Figure A.4 shows the simulated trap occupation distribution (empty trap distribution) for the MESFET with SI substrate traps only for  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  for the forward curve as  $V_{DS}$  rises (solid curve) and the return curve as  $V_{DS}$  falls (dashed curve). The acceptor trap concentration for the simulation is  $1 \times 10^{17} \text{ cm}^{-3}$  and the trap distribution starts from  $y = 0.3 \text{ }\mu\text{m}$  from the device surface and is evenly distributed in the substrate. Figure A.4 actually is a plot of the concentration of empty (unoccupied by electrons) trap centers under the gate along the center of the gate at  $V_{DS} = 19 \text{ V}$  as rises (forward curve) and falls (return curve). Figure A.4 further shows that the trapping and detrapping of electrons largely occurs on the substrate side of the channel-substrate interface as widely reported in the literature, although on the return curve we see that

trapping also occurs in the substrate during capture dominant phase as  $V_{DS}$  falls. Figure A.4 shows that, on the forward curve as  $V_{DS}$  rises, there are more unoccupied (empty) trap centers, and hence fewer trapped electrons due to the emission-dominant process. On the return curve, however, as  $V_{DS}$  falls, due to the capture dominant process, there are fewer empty (unoccupied) trap centers since in this case more electrons have been captured. We also observe that on the return curve the electron trapping extends more into the substrate due to the capture dominant process than on the forward curve where emission is the dominant process. The electron capture dominant process as  $V_{DS}$  falls and the electron emission dominant process as  $V_{DS}$  rises lead to lower free electron concentration on the return curve as  $V_{DS}$  falls than on the forward curve as  $V_{DS}$  rises, as shown in Figure A.5. This in turn leads to a lower electron current as  $V_{DS}$  falls (return curve) than when  $V_{DS}$  rises (forward curve) as shown in Figure A.6, leading to the hysteresis (looping) in the drain I-V characteristics as  $V_{DS}$  rises and falls.

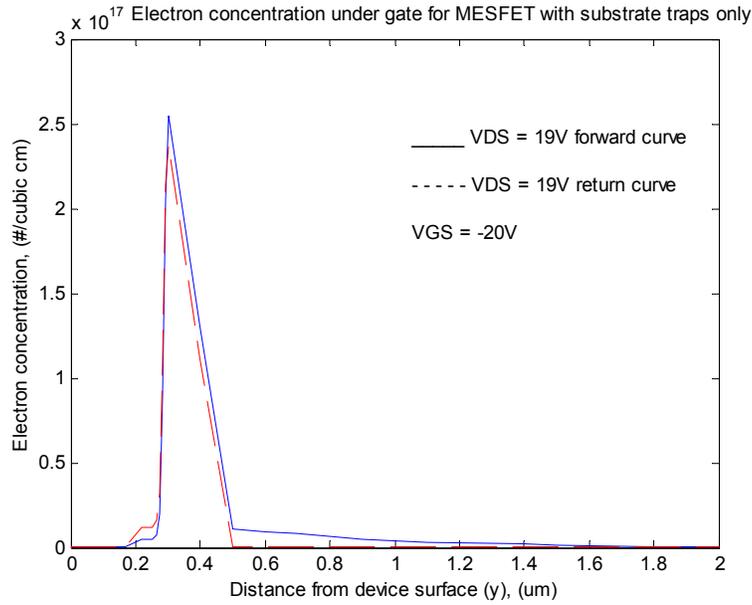


Figure A.5: Electron concentration under the gate for MESFET with substrate traps only for  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  for the forward curve (solid curve) and return curve (dashed curve).

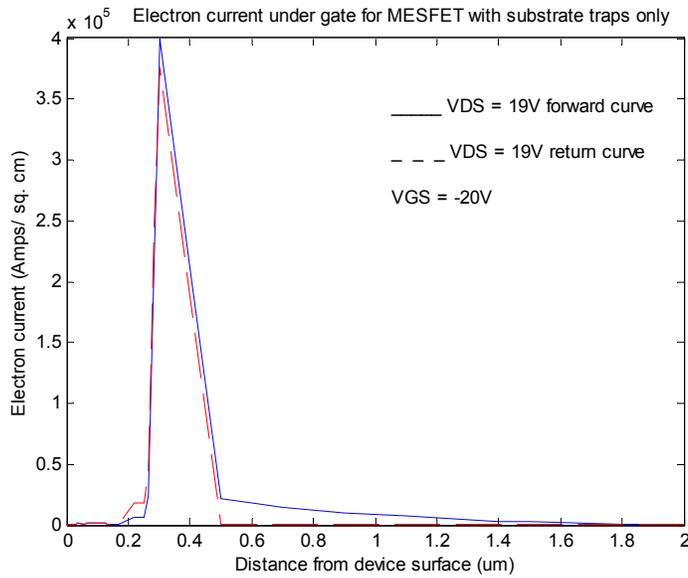
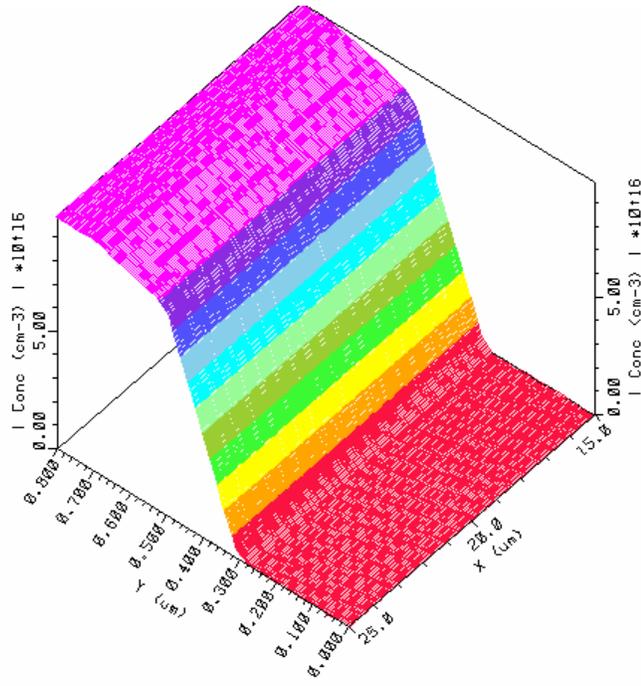
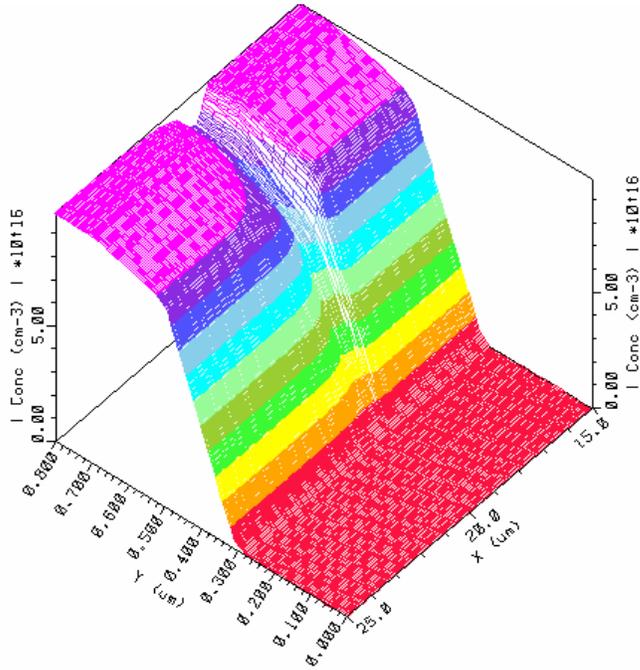


Figure A.6: Current under the gate for MESFET with substrate traps only for  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  for the forward curve (solid curve) and return curve (dashed curve).



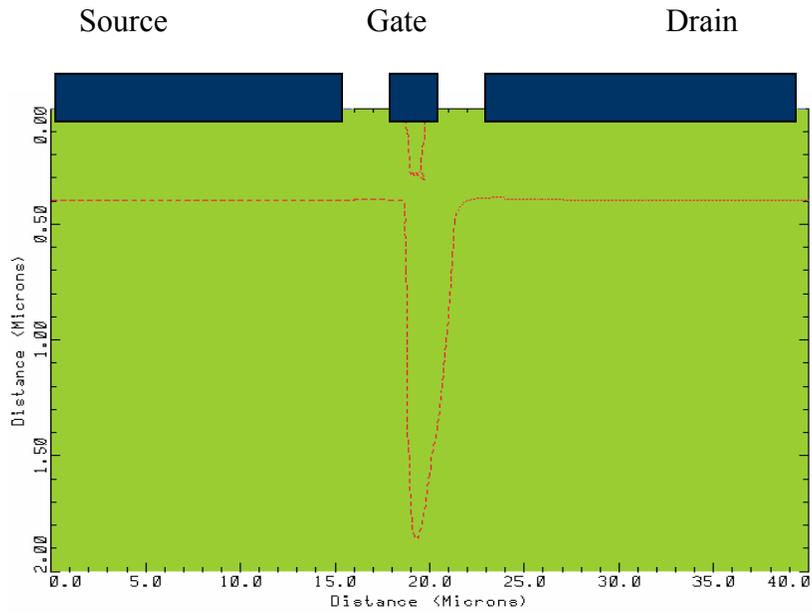
(a)



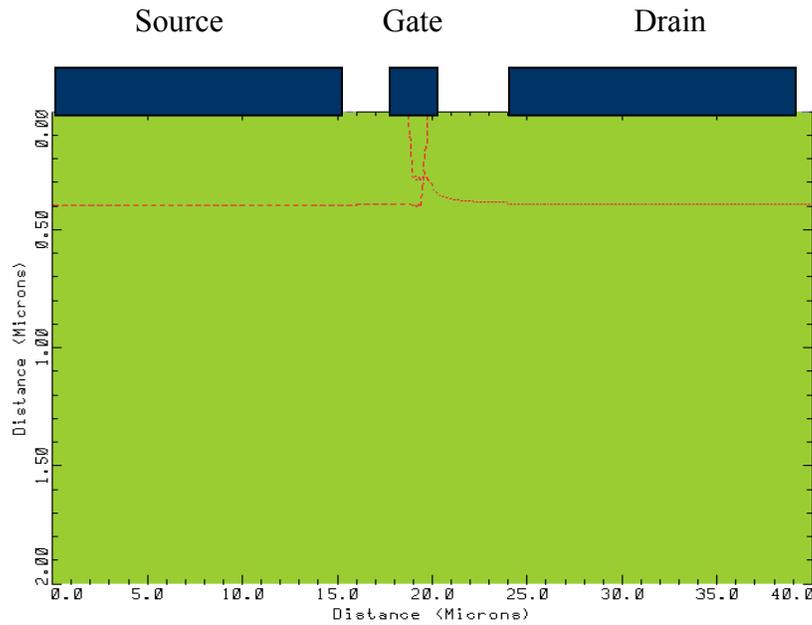
(b)

Figure A.7: 3-D empty trap distribution for MESFET with only substrate traps at  $V_{DS}=19$  V (a) on the forward I-V curve (b) on the return I-V curve.  $V_{GS} = -20$  V.

Figures A.5 and A.76 indicate that the trapping and emission processes occur at the substrate side of the channel-substrate interface as widely reported in the literature, and Figures A.7(a) and A.7(b) show that the trapping and emission processes occur largely under gate and in the vicinity of the gate on the substrate side of the interface. The band diagram for the return curve further shows that the depletion region at the channel-substrate interface on the substrate side is wider (i.e. extends more into the channel) than it is for the forward curve. Hence, the channel is narrower (more constricted) for the return curve than for the forward curve. This is evident in Figures A.8a and A.8b, in which the depletion regions at  $V_{DS} = 19$  V for the forward and return curves are shown respectively. Both figures show the depletion region under the gate due to the gate Schottky barrier and the edge of the depletion region due to substrate traps. Figure A.8a for the forward curve shows a wide separation between the gate and substrate depletion regions, indicating a wider channel.



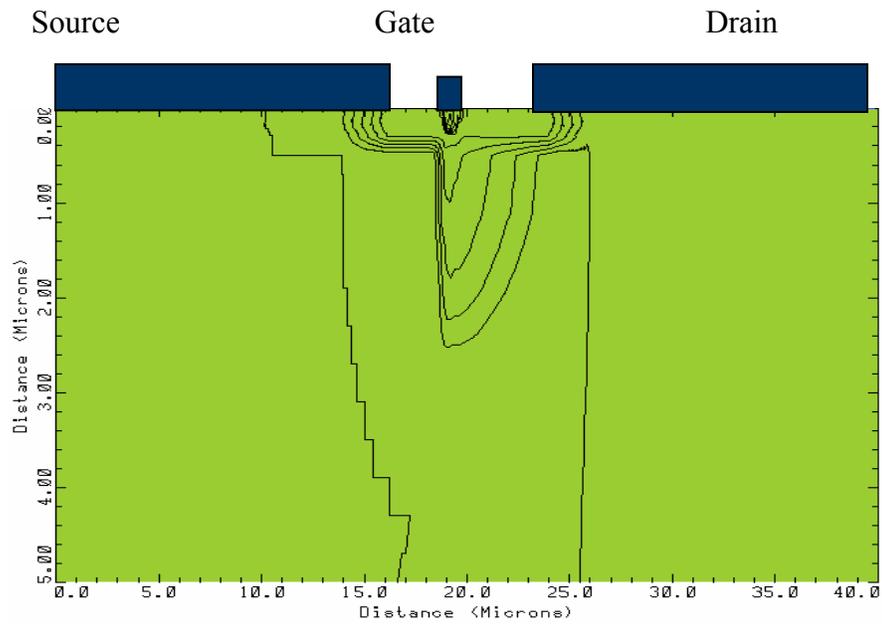
(a)



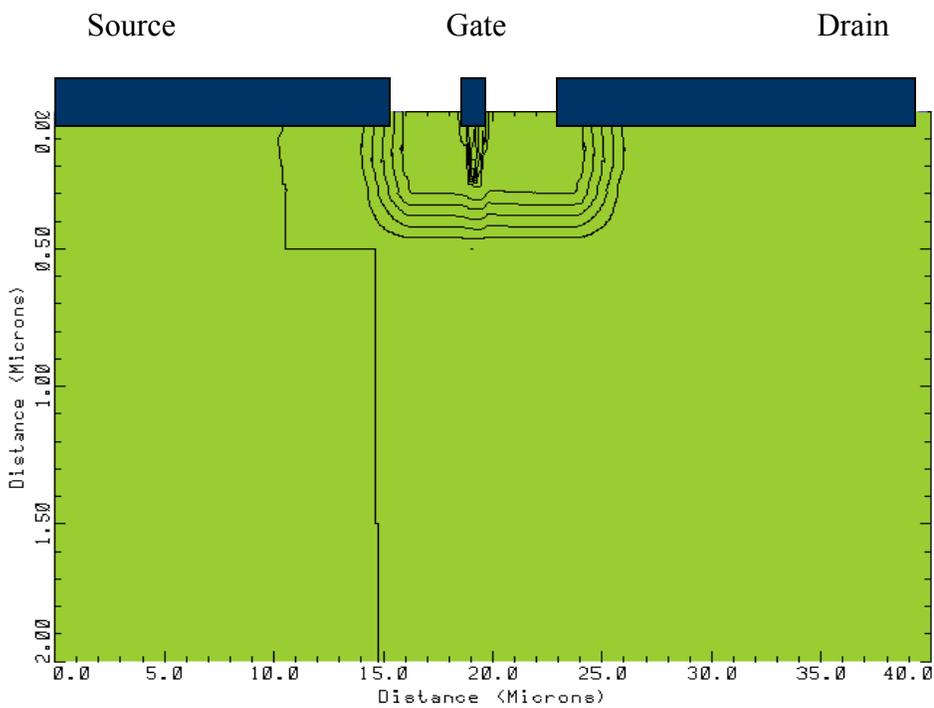
(b)

Figure A.8: Depletion regions for MESFET with substrate traps only for (a)  $V_{DS}=19$  V on the forward curve and (b)  $V_{DS}=19$  V on the return curve.  $V_{GS} = -20$  V.

Figure A.8(b) for the return curve, however, shows that the gate and substrate depletions virtually touch under the gate, constricting the channel under the gate. This is due to the fact that on the return curve, as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V, more electrons are trapped at the channel-substrate interface and the depletion region due to the trapped electrons encroaches upon the channel reducing the channel thickness, particularly under the gate. Due to the wider channel indicated in Figure A.8(a) lower potential barrier shown in Figure A.3 on the forward curve, Figure A.9(a) shows that the current is more widespread for  $V_{DS}=19$  V for the forward curve leading to large amounts of substrate current. The narrower channel in Figure A.8(b) and higher potential barrier on the return curve in Figure A.3 lead to the current being restricted mainly to the channel and channel-substrate interface as shown in Figure A.9(b) for the current contours for  $V_{DS}=19$  V for the return curve.



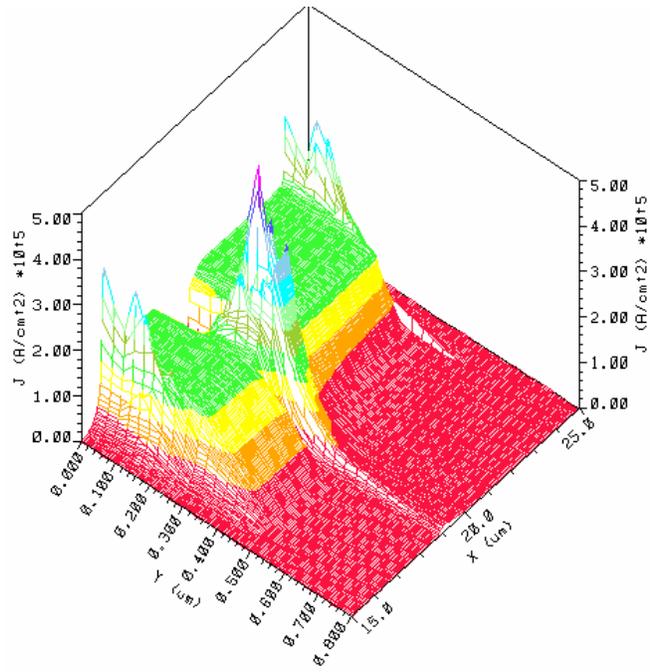
(a)



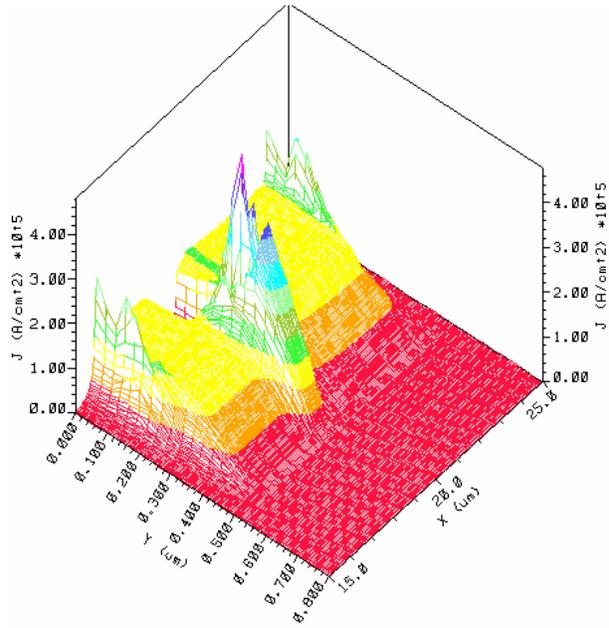
(b)

Figure A.9: Current contours for MESFET with substrate traps only for  $V_{DS} = 19$  V  
 (a) on the forward curve (b) on the return curve.  $V_{GS} = -20$  V.

As a result, the free electron concentration and therefore the current are lower for the return curve than they are for the forward curve as shown in Figures A.5 and A.6, leading to the hysteresis (looping) in the drain I-V characteristics. It should be noted that electron capture and emission are dynamic processes and that the diagrams shown in Figures A.1 to A.9 only capture one instance in time. Figures A.10 (a) and A.10 (b) show the 3-D current plots for  $V_{DS}=19V$  on the forward and return curves respectively. The return current distribution is generally lower than the forward current distribution as indicated by the scale and color map, in which red has the lowest magnitude and violet has the highest magnitude as in the electromagnetic spectrum.



(a)



(b)

Figure A.10: Electron current for MESFET with substrate traps only at  $V_{DS}=19$  V for (a) the forward curve for  $V_{GS}=-20$  V. Note the green patches, indicating relatively higher current. (b) the return curve for  $V_{GS}=-20$  V. Note the yellow patches, indicating relatively lower current.

It can be observed from the above analysis that, there seem to be two mechanisms responsible for hysteresis in MESFETs with substrate traps. One mechanism is the capture of channel electrons by deep level traps at the substrate side of the channel-substrate interface under the gate and in the vicinity of the gate. As a result, the channel electron concentration as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V (return curve) is less, due to electron capture, than the channel electron concentration as  $V_{DS}$  rises from 0 V to  $V_{DS(max)}$ , due to electron emission (forward curve), for a given  $V_{DS}$ , thus contributing to the hysteresis in the drain I-V curve. The other contributing mechanism is manifested as follows. Neutral (empty) deep level acceptor traps on the substrate side of the channel-substrate interface trap channel electrons and become negatively charged. Here we note that the deep level traps are immobile and therefore we end up with immobile negatively charged (ionized) deep level acceptors at the substrate side of the channel-substrate interface. This increases the potential barrier at the channel-substrate interface in accordance with Poisson's equation (the Poisson law), and increases the depletion region width at the interface as the ionized negative deep acceptors repel channel electrons. This, coupled with the depletion region under the gate due to the gate Schottky barrier, constricts the channel as indicated by the band diagram for the return curve, leading to reduced drain-source current as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V [16] and therefore hysteresis in the drain I-V characteristics.

## A.2 MESFET with Source/Drain Implant Damage Traps only

Figure A.11 shows the simulated drain I-V characteristics of a MESFET with traps representing source/drain residual implant damage traps only in the channel. For the simulation of MESFET with traps representing source/drain residual implant damage traps only, the n-channel device is built on a p-type substrate. There is therefore a large potential barrier at the channel-substrate interface, restricting the current mainly to channel so that effects of the implant damage traps can be studied. The implant damage trap concentration used in the simulation is  $1.5 \times 10^{17} \text{ cm}^{-3}$  with the distributed energy levels and the trap spatial distribution extends from  $x = 0 \text{ }\mu\text{m}$  to  $x = 16.5 \text{ }\mu\text{m}$  on the source side and  $x = 23.5 \text{ }\mu\text{m}$  to  $x = 40 \text{ }\mu\text{m}$  on the drain side. The depth of the trap distribution at both the source and drain sides is  $0.4 \text{ }\mu\text{m}$  from the device surface (i.e.,  $y = 0.4 \text{ }\mu\text{m}$ ). Here we note that the dimensions of the source and drain  $n^+$  ohmic contact regions are  $x = 16 \text{ }\mu\text{m}$  by  $y = 0.2 \text{ }\mu\text{m}$ .

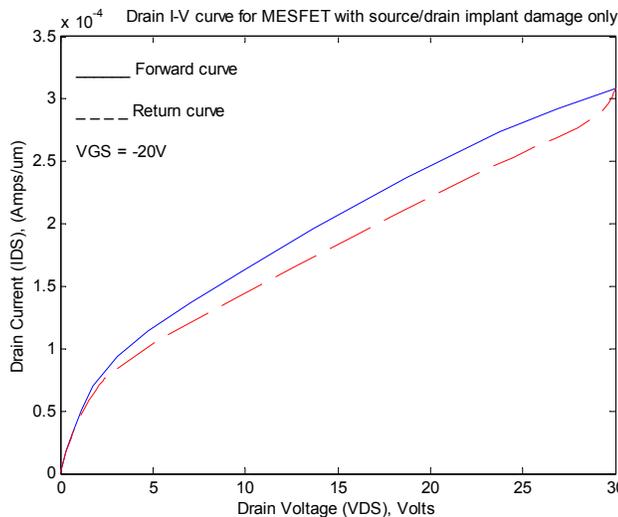
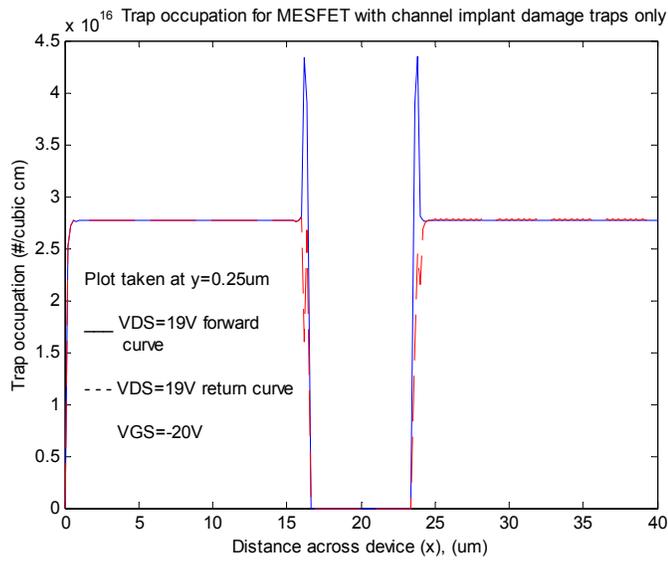
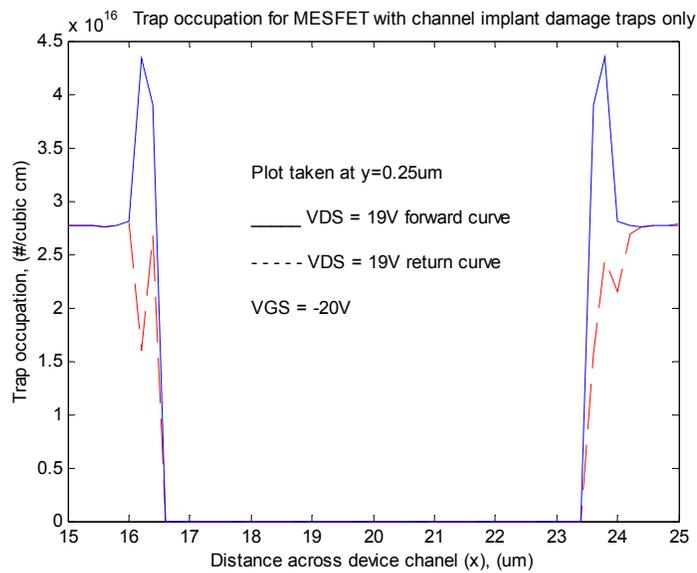


Figure A.11: Drain I-V characteristics for MESFET with source/drain residual implant damage traps only.

For the MESFET with source/drain residual implant damage traps only, Figure A.12 shows that the trapping and emission processes take place largely in the pencil of traps at the un-gated inside edges of the source and drain regions due to the lateral straggle (standard deviation) of implanted ions. These regions extend from 16.00  $\mu\text{m}$  to 16.50  $\mu\text{m}$  at the source side and 23.50  $\mu\text{m}$  to 24.00  $\mu\text{m}$  at the drain side for our simulations. The lateral straggle is formed because of the statistical nature of the implantation process, leading to the implanted ions being scattered laterally and penetrating past the edges of the implant mask [59]. The lateral straggle is formed in addition to the vertical straggle, resulting in a 2-dimensional profile. Simulations show that the hysteresis in the drain I-V characteristics for MESFET with source/drain residual implant damage traps only is due to the pencil of traps that results from the lateral straggle at the source and drain regions. No hysteresis is seen in the simulated drain I-V characteristics when the traps due to lateral straggle are reduced to zero, as will be shown later.



(a)

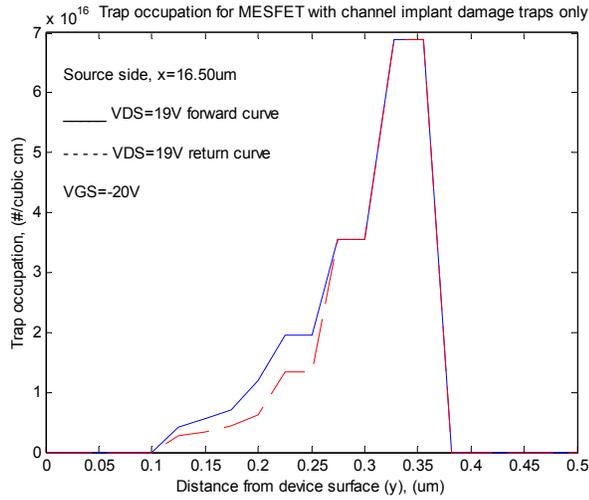


(b)

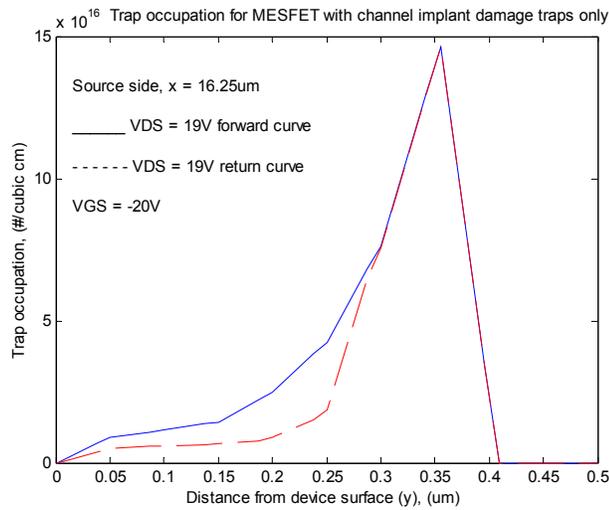
Figure A.12: (a) Trap occupation (empty, unoccupied trap centers) distribution across the channel for MESFET with source/drain residual implant damage traps only. (b) An expanded plot.

Figure A.13 shows the 1-D trap occupation (empty, unoccupied trap centers) at distances of  $x = 16.25 \mu\text{m}$  and  $16.50 \mu\text{m}$  at the source side and Figure A.14 shows the 1-D trap occupation (empty, unoccupied trap centers) at  $x = 23.50 \mu\text{m}$  and  $23.75 \mu\text{m}$  at the drain side. Both figures show that the concentration of unoccupied (empty) trap centers on the return curve ( $V_{\text{DS}}$  falling from  $V_{\text{DS(max)}}$  to 0 V) is less than that on the forward curve ( $V_{\text{DS}}$  rising from 0 V to  $V_{\text{DS(max)}}$ ) for a given  $V_{\text{DS}}$  at both the source and drain sides. This means that as  $V_{\text{DS}}$  falls, due to the capture dominant process, there are more electrons captured than on the forward curve (rising  $V_{\text{DS}}$ ) where electron emission dominates, as already observed above. On the other hand, as  $V_{\text{DS}}$  rises, due to the emission-dominant process, the concentration of electrons captured is less than (more unoccupied, empty, trap centers) on the return curve (falling  $V_{\text{DS}}$ ) where electron-capture dominates. Figures A.15a and A.15b show the 3-D trap occupation for MESFET with traps simulating only source/drain residual implant damage at  $V_{\text{DS}}=19\text{V}$  for the forward and return curves respectively. A comparison of the figures indicates that the trapping and emission processes take place mainly in the pencil or volume of traps due to lateral straggle of implanted ions, as already suggested. Figure A.15b further shows that capture is the dominant process as  $V_{\text{DS}}$  falls from  $V_{\text{DS(max)}}$  to 0 V, since the concentration of unoccupied trap centers is lower due to increased electron capture. There is no change in trap occupation outside the lateral straggle areas between the forward and return curves for given  $V_{\text{DS}}$  as shown in Figures A.12 and A.15. Thus, although trapping occurs at the channel side of the channel-substrate interface as shown in Figure A.14, it is the trapping and emission processes that take place in the pencil or volume of traps due to the lateral

straggle of implanted ions that lead to the hysteresis in the drain I-V characteristics for MESFET with traps representing source-drain residual implant damage traps only.

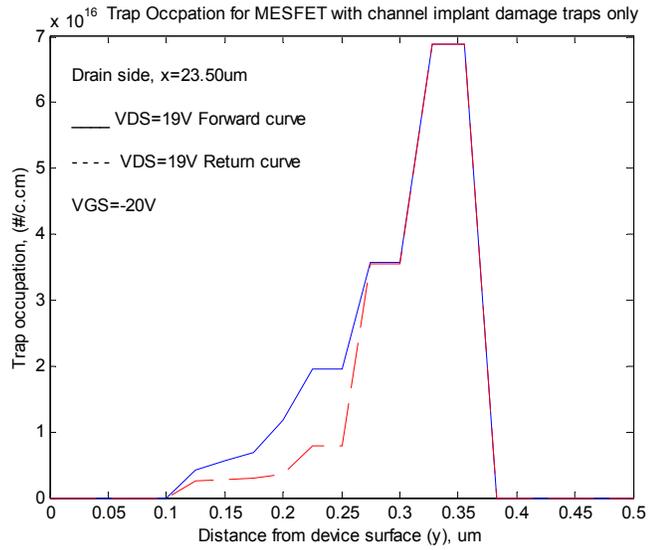


(a)

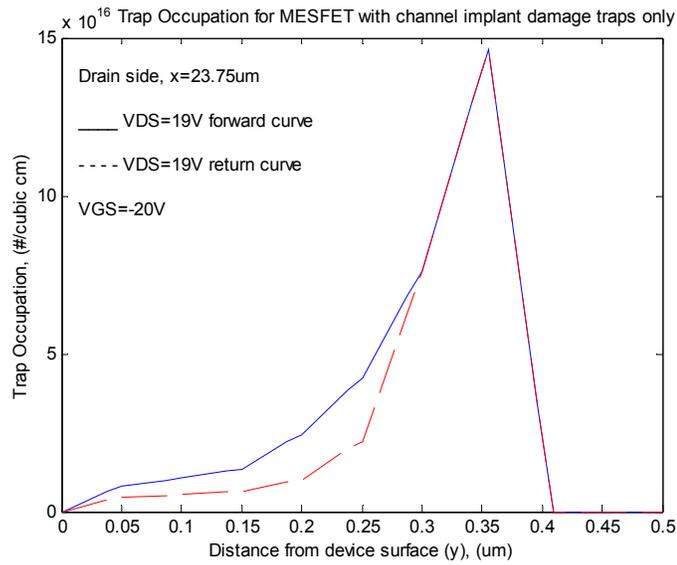


(b)

Figure A.13: Trap occupation (empty, unoccupied trap centers) distribution for MESFET with source/drain residual implant damage traps only at the source side (a) with  $x = 16.5 \mu\text{m}$  and (b) with  $x = 16.25 \mu\text{m}$ .

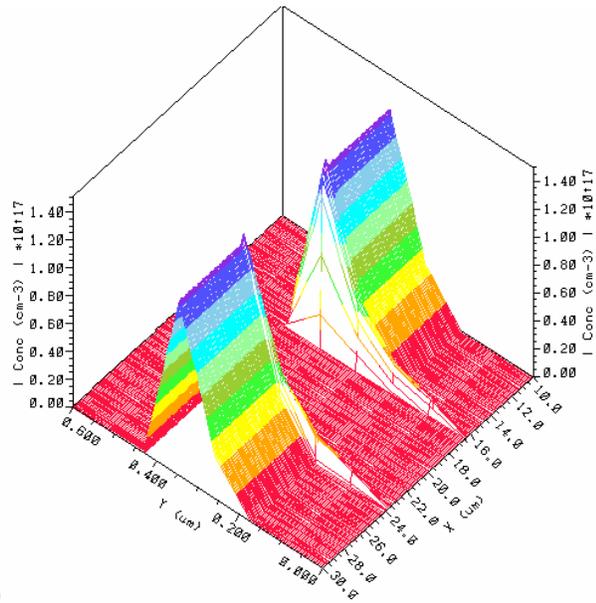


(a)

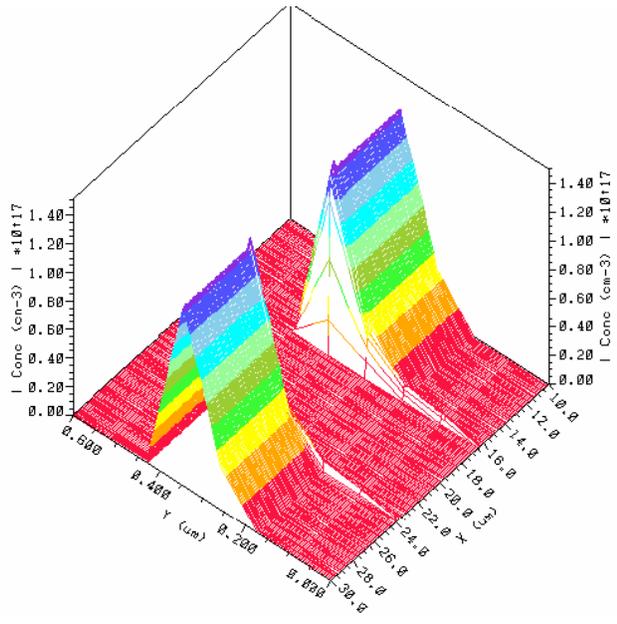


(b)

Figure A.14: Trap occupation (empty, unoccupied trap centers) distribution for MESFET with source/drain residual implant damage traps only at the drain side (a) with  $x = 16.5 \mu\text{m}$  and (b) with  $x = 16.25 \mu\text{m}$ .



(a)



(b)

Figure A.15: Trap occupation (empty, unoccupied trap centers) for MESFET with source/drain residual implant damage only for (a)  $V_{DS}=19$  V on the forward curve. Note the pencil of traps where most trapping and emission occur. (b)  $V_{DS}=19$  V on the return curve. Note the reduction in unoccupied trap concentration in the pencil of traps due to trapping

Figure A.16 shows the drain I-V characteristics of a MESFET with source/drain residual implant damage traps only but no traps due to lateral straggle implant damage. No hysteresis occurs in the simulated drain I-V characteristics as already pointed. Figure A.17 shows the 1-D empty trap distribution across the channel at 0.25  $\mu\text{m}$  below the device surface ( $y = 0.25 \mu\text{m}$ ) at  $V_{DS} = 19 \text{ V}$  on the forward and return curves, and  $V_{GS} = -20 \text{ V}$ . This is the same location as the empty trap distribution plot shown in Figure A.12. As can be seen, the trap occupation (empty trap distribution) is the same for both the forward and return curves, and there are no trapping and detrapping processes taking place in the pencil of traps due to lateral straggle as the lateral straggle and its attendant traps have been reduced to zero, unlike the situation shown in Figure A.12.

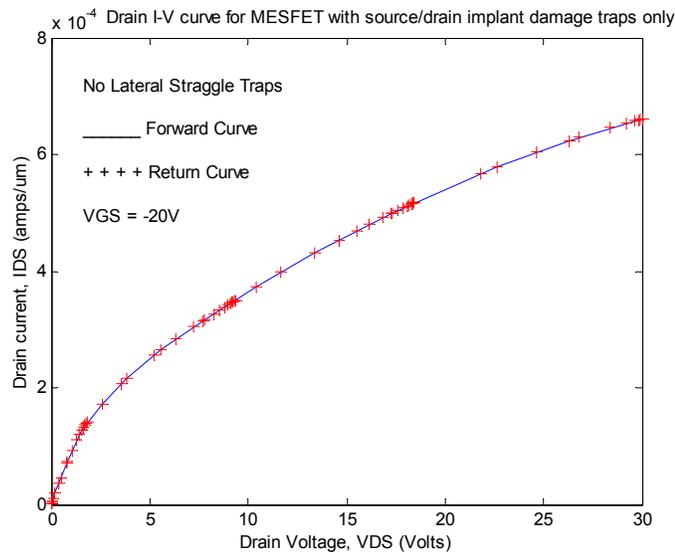


Figure A.16: Drain I-V characteristics for MESFET with source/drain residual implant damage traps only with traps due to lateral straggle of implanted ions reduced to zero. Note the absence of hysteresis in the I-V curve compared to Figure A.11. Also note the increase in current compared to Figure A.11 due to reduced trapping of channel electrons and reduction in channel resistance due to trapped electrons.

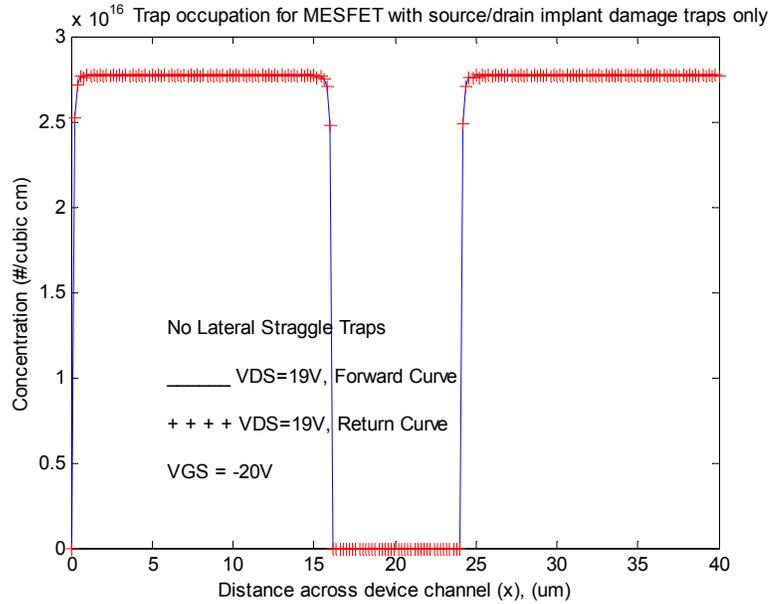
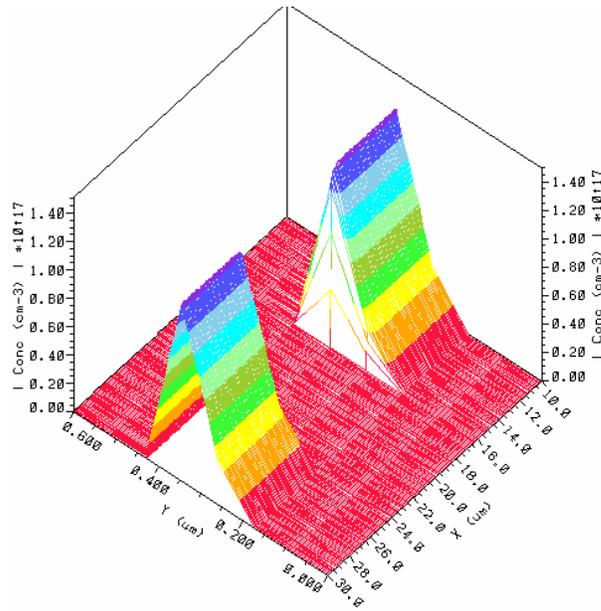
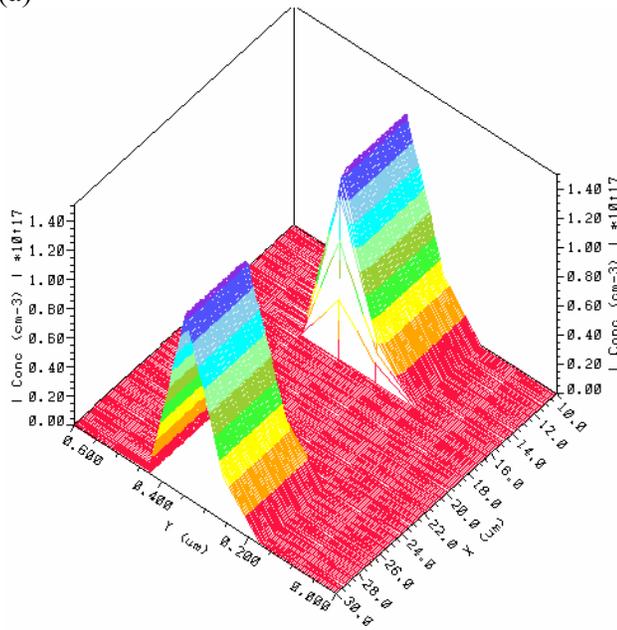


Figure A.17: 1-D trap occupation across device channel for MESFET with source/drain residual implant damage traps only. Note the absence of traps due to lateral straggle compared to the situation in Figure A.11.

Figure A.18 further shows the 3-D trap occupation (empty traps) at  $V_{DS} = 19 \text{ V}$  on the forward and return curves for  $V_{GS} = -20 \text{ V}$ . Again, the empty trap distribution is the same for the forward and return curves. The regions of trap occupation due to the lateral straggle of implanted species are absent compared to the situation depicted in Figure A.15. Figure A.19 indicates that the 3-D current distribution at  $V_{DS} = 19 \text{ V}$ ,  $V_{GS} = -20 \text{ V}$  is the same for both the forward and return curves leading to the absence of hysteresis in the drain I-V characteristics. This is due to absence of capture and emission processes that take place in the volume of traps due to lateral straggle of implanted species.

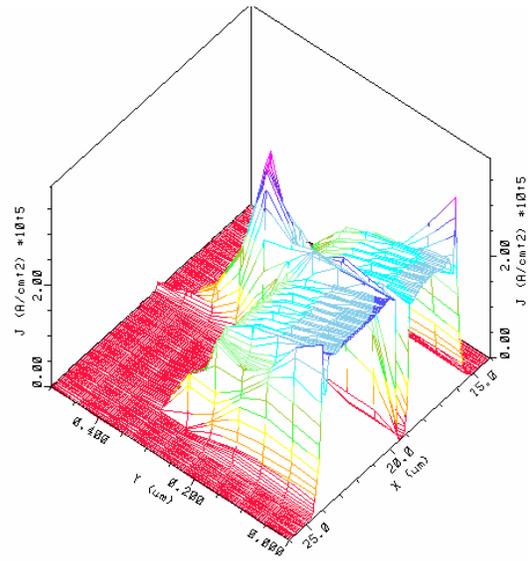


(a)

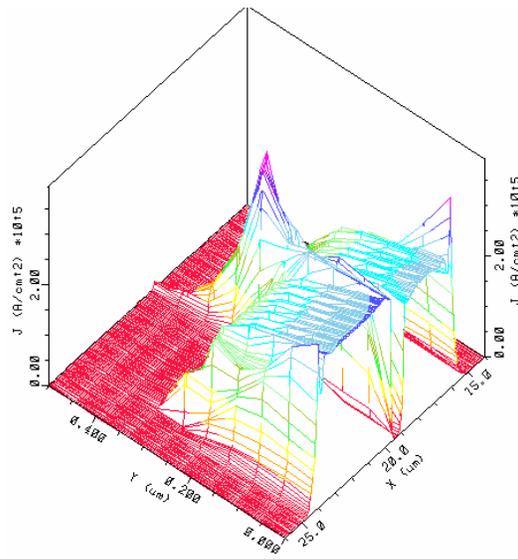


(b)

Figure A.18: 3-D trap occupation (empty, unoccupied trap centers) for MESFET with source/drain residual implant damage traps only without traps generated by lateral straggle of implanted ions at  $V_{DS}=19$  V,  $V_{GS} = -20$  V for (a) forward curve and (b) return curve. Note the absence of traps due lateral straggle compared to Figure A.15.



(a)



(b)

Figure A.19: 3-D current distribution for MESFET with source/drain residual implant damage traps only without traps generated by lateral straggle of implanted ions at  $V_{DS}=19$  V,  $V_{GS} = -20$  V for (a) forward curve and (b) return curve. Note that the current distributions are the same for the forward and return curves.

The fact that the trapping and detrapping, and therefore hysteresis occurs mainly in the pencil of traps due to the lateral straggle of implanted ions at un-gated regions of the inside edges of the source and drain is because the current mainly flows between the right edge of the source and left edge of the drain in the channel, as shown in Figure A.20 below. Figures A.21a and A.21b show the 3-D current plots which also confirm that the current flow is mainly restricted to the channel in the region between the inside edges of the source and drain.

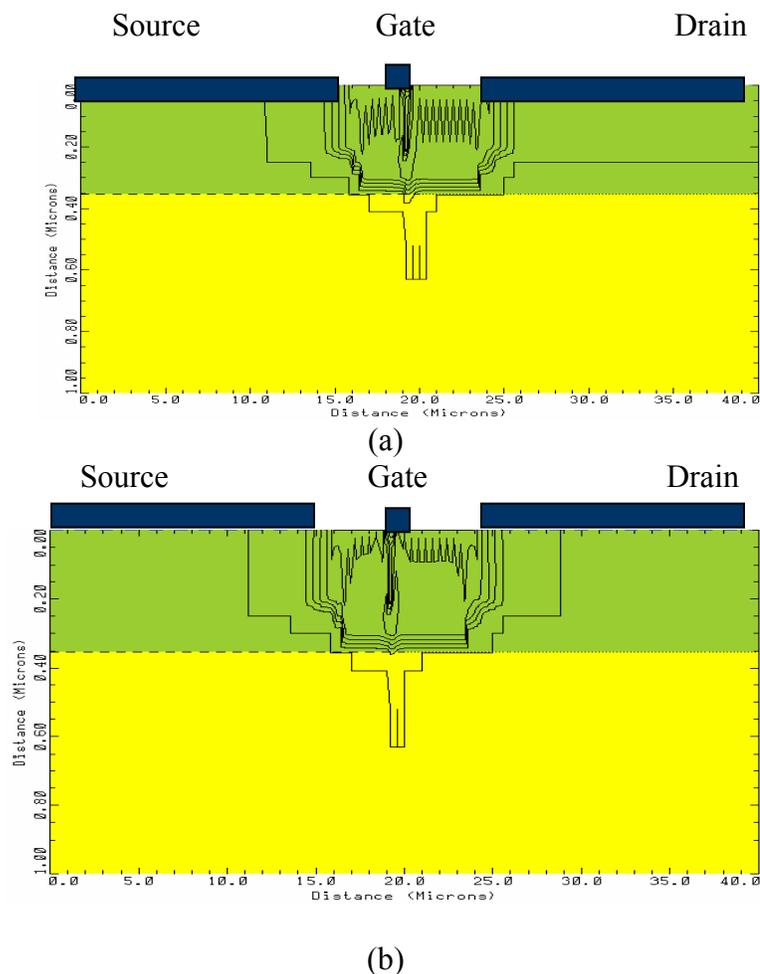


Figure A.20: 2-D Current contours for MESFET with source/drain implant damage traps only at  $V_{DS}=19$  V for (a) forward curve and (b) return curve.  $V_{GS} = -20$  V.

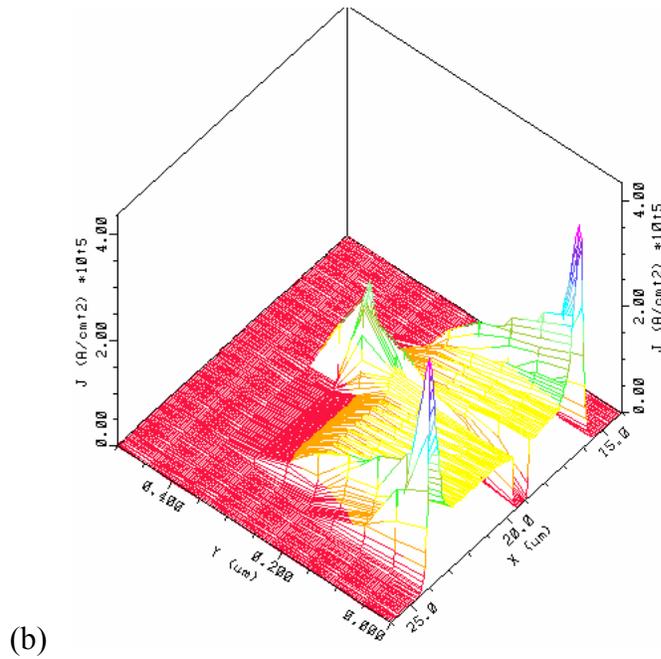
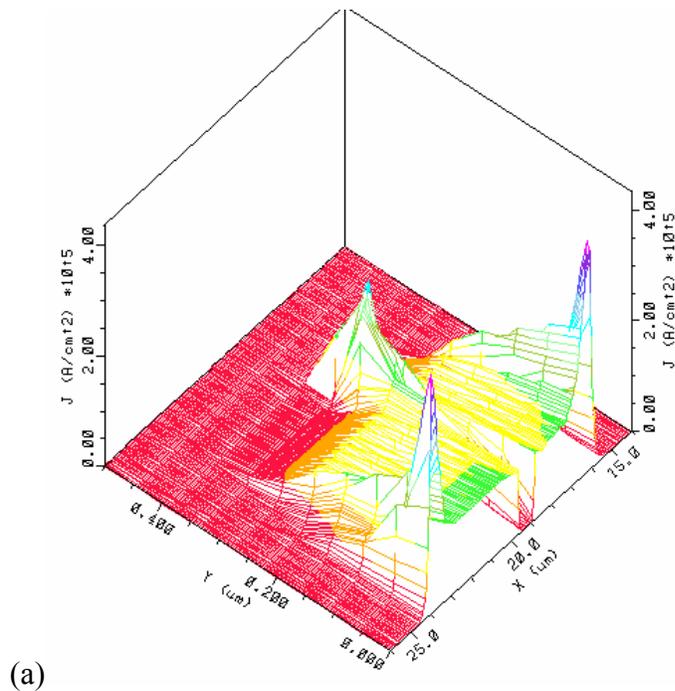
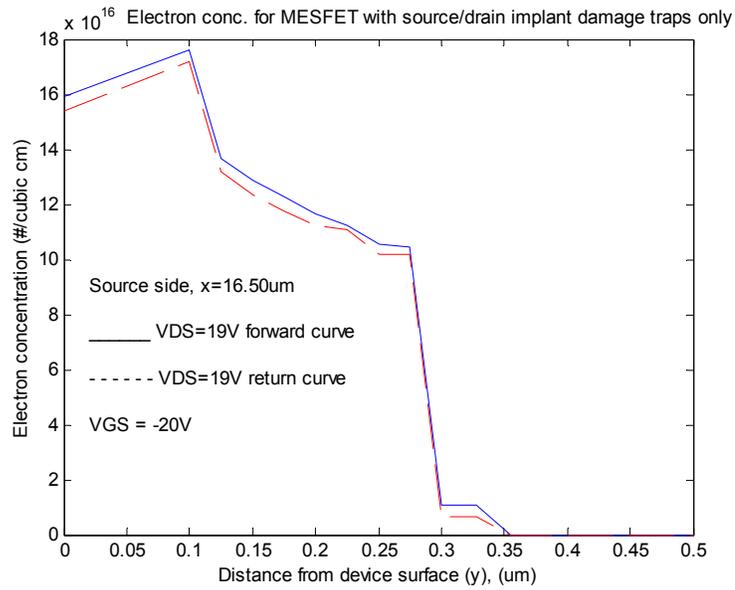
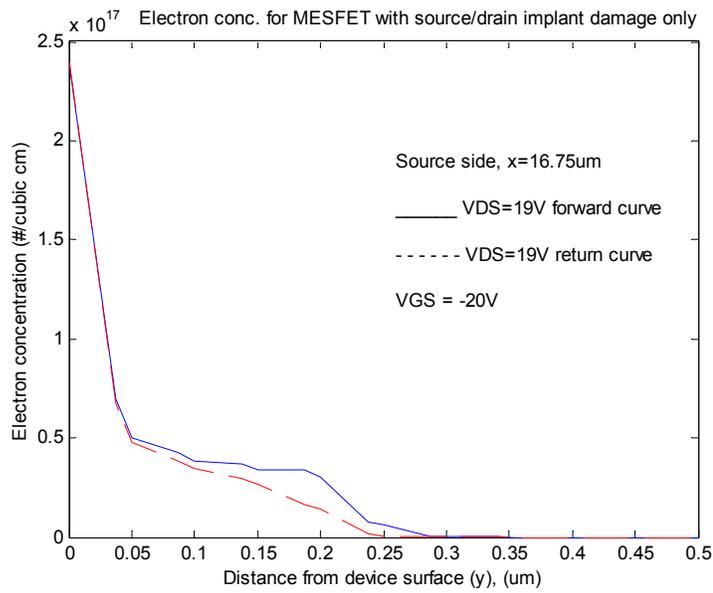


Figure A.21: 3-D Current plots for MESFET with source/drain implant damage traps only at  $V_{DS}=19$  V for (a) forward curve. Note the presence of green patches. (b) return curve. Note the reduction of green patches. This is an indication of lower current.  $V_{GS} = -20$  V.

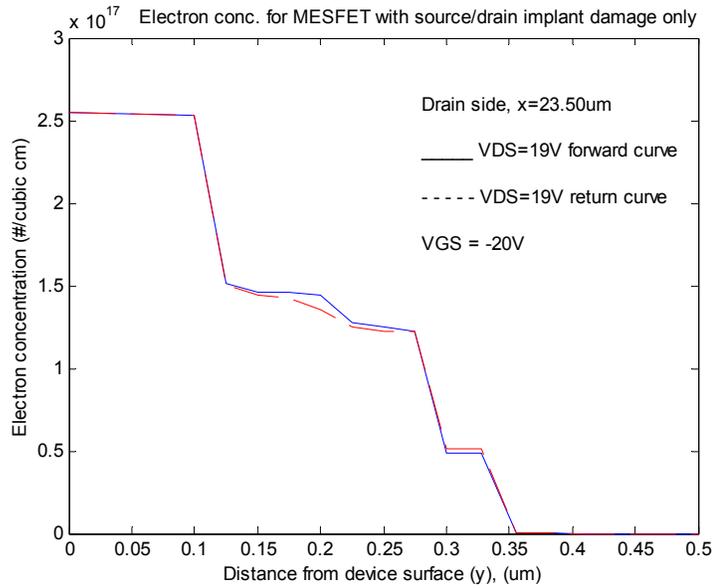


(a)

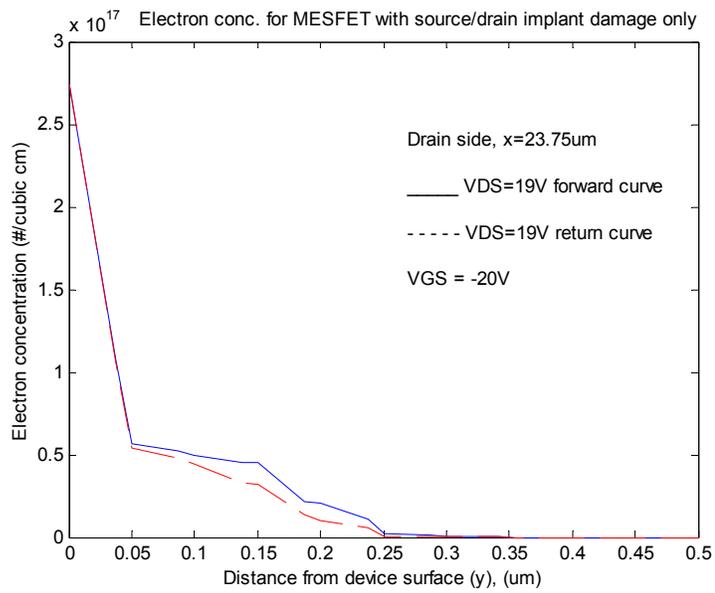


(b)

Figure A.22: Electron concentration distribution for MESFET with source/drain residual implant damage traps only at the source side for (a)  $x = 16.5 \mu\text{m}$  (b)  $x = 16.75 \mu\text{m}$ .

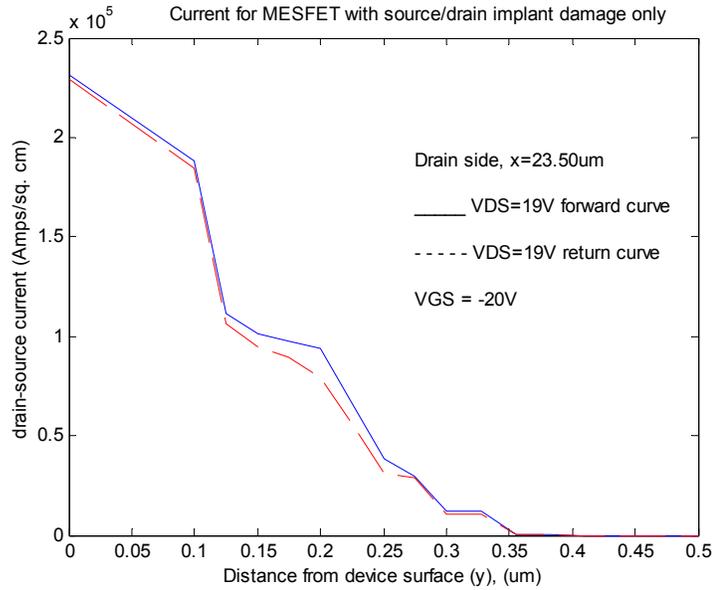


(a)

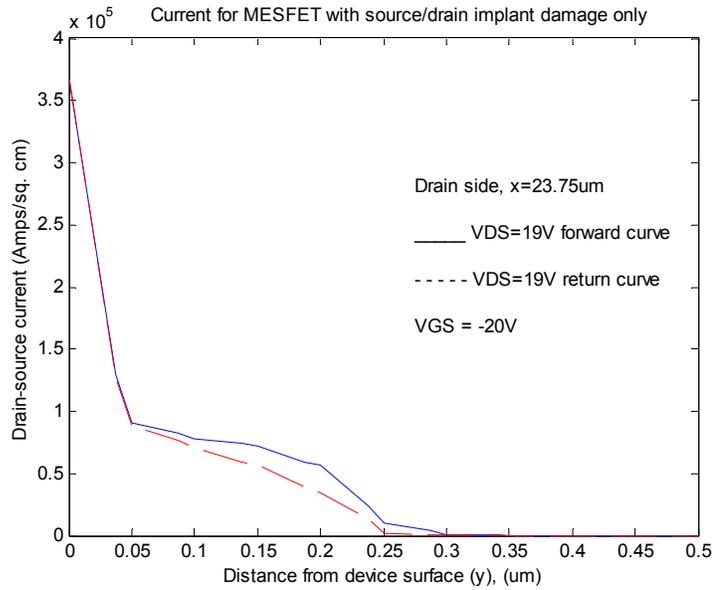


(b)

Figure A.23: Electron concentration distribution for MESFET with source/drain residual implant damage traps only at the drain side for (a)  $x = 23.5 \mu\text{m}$  and (b)  $x = 23.75 \mu\text{m}$ .



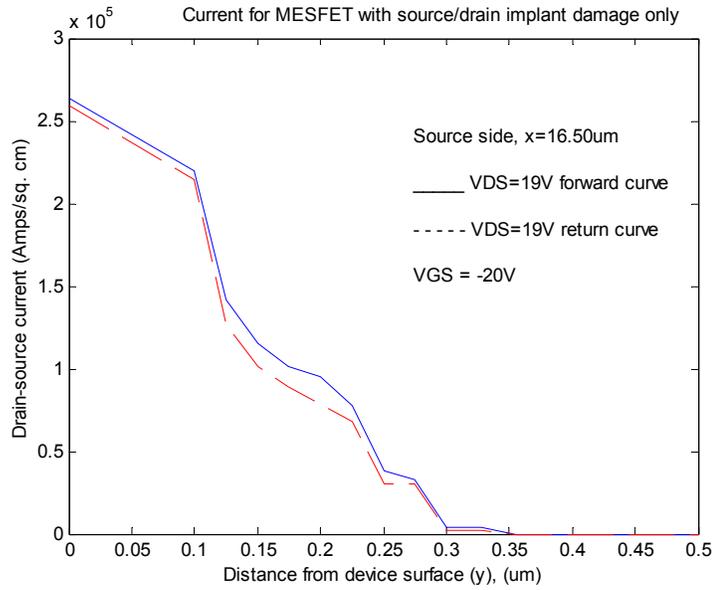
(a)



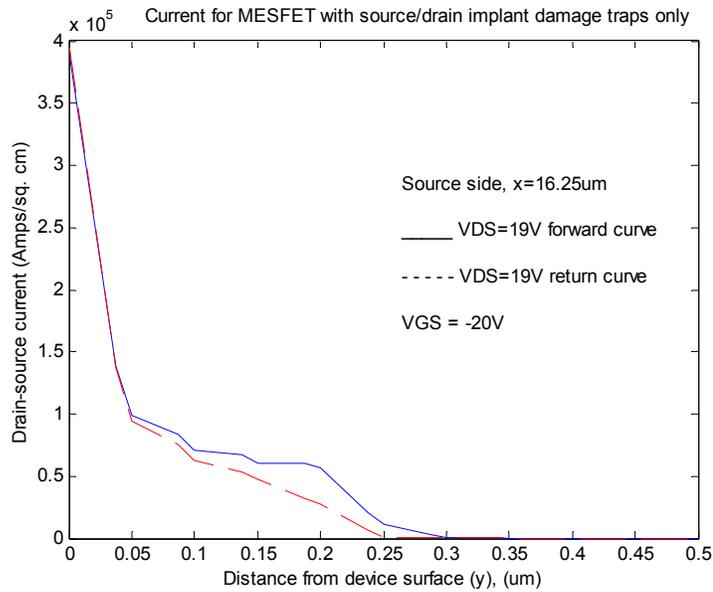
(b)

Figure A.24: Drain-source current distribution for MESFET with source/drain residual implant damage traps only at the drain side for (a)  $x = 23.5 \mu\text{m}$ . (b)  $x = 23.75 \mu\text{m}$ .

Figures A.22 to A.25 show that the 1-D electron concentration and therefore current distributions for the return curve are lower than those for the forward curve for the same  $V_{DS}$ , leading to the hysteresis (looping) in the drain I-V characteristics. As already mentioned else above, it is the difference in trap occupation as  $V_{DS}$  rises and falls that leads to the difference in free electron concentration and electron current distribution, and hence in the difference in drain current as  $V_{DS}$  rises and falls that result in the hysteresis in the drain I-V characteristics. If there is no difference in trap occupation as  $V_{DS}$  rises and falls for given  $V_{GS}$ , there will be no difference in free electron concentration and electron current distribution as  $V_{DS}$  rises and falls, as already mentioned. There will therefore be no difference in the drain current as  $V_{DS}$  rises and falls and hence, no hysteresis (looping) in the drain I-V characteristics.



(a)



(b)

Figure A.25: Drain-source current distribution for MESFET with source/drain residual implant damage traps only at the source side at (a)  $x = 16.50 \mu\text{m}$  (b)  $x = 16.25 \mu\text{m}$ .

From the above treatment we observe that hysteresis in a device with traps representing source/drain residual implant damage traps only in the channel area is due to capture and emission processes in the trap region representing lateral straggle traps. To further investigate the physics behind the hysteresis in the drain I-V curves of a MESFET with channel traps representing implant damage traps, we simulate a device with implant damage traps obtained by Dalibor et al. [33] after He<sup>+</sup>-implantation since these traps are intrinsic. The traps have energy levels (activation energies) of  $E_C - E_t = 1.545$  eV,  $E_C - E_t = 1.03$  eV,  $E_C - E_t = 0.93$  eV,  $E_C - E_t = 0.655$  eV,  $E_C - E_t = 0.33$  eV, and  $E_C - E_t = 0.2$  eV. The traps are restricted to the areas on the source and drain sides representing the lateral straggle with a width = 0.6  $\mu\text{m}$  and depth = 0.3  $\mu\text{m}$  with total trap concentration of  $2.0 \times 10^{17} \text{ cm}^{-3}$ . We used a 30V symmetric triangular pulse with a pulse width of 30 s. Thus it takes 15 s for  $V_{DS}$  to go from 0 V to 30 V and 15 s to go back to 0 V.

Figure A.26 shows the band diagrams for  $V_{DS} = 0$  V,  $t = 0$  s;  $V_{DS} = 30$  V,  $t = 15$  s; and  $V_{DS} = 0$  V,  $t = 30$  s taken along the trap region on the source side. The band diagram shows that at  $t = 0$  s,  $V_{DS} = 0$  V due to trapping of channel electrons the material is relatively compensated and as already mentioned above, emission is the dominant process. As  $V_{DS}$  increases towards  $V_{DS(\text{max})}$  the emission-dominant process gradually gives way to a capture-dominant process. The band diagram at  $V_{DS} = V_{DS(\text{max})} = 30$  V,  $t = 15$  s suggests that due to the emission process the free electron density in the conduction band is relatively higher than at  $t = 0$  s since the Fermi level ( $E_f$ ) is closest to the conduction band edge ( $E_C$ ). This indicates that capture is the dominant process since there is relatively a large quantity of electrons present. Since the emission time constant

is relatively much longer the capture time constant, the trapped electrons remain trapped as  $V_{DS}$  decreases from  $V_{DS(max)} = 30$  V back towards  $V_{DS} = 0$  V,  $t = 30$  s and more electrons are captured as  $V_{DS}$  continues to decrease towards  $V_{DS} = 0$  V. The band diagram at  $V_{DS} = 0$  V,  $t = 30$  s shows that due to excessive trapping as  $V_{DS}$  decreases back to 0 V the material becomes more compensated than at  $V_{DS} = 0$  V,  $t = 0$  s since  $E_f$  is closer to mid-gap than at  $t = 0$  s. At  $V_{DS} = 0$  V,  $t = 30$  s emission is again the dominant process since maximum trapping has been achieved and there is a minimum number of free electrons present. Thus the only process that can take place is emission. Figure A.27 shows a similar scenario along the trap region on the drain side. From Figure A.28 we observe that at  $V_{DS} = 0$  V,  $t = 0$  s due to the emission dominant process there is relatively a high concentration of empty traps and at  $V_{DS} = 30$  V,  $t = 15$  s due to the capture dominant process the concentration of empty traps is lowest. As already mentioned above, as  $V_{DS}$  falls back from 30 V to 0 V, the capture-dominant process gradually gives way to an emission dominant process. As a result at  $V_{DS} = 0$  V,  $t = 30$  s the concentration of empty traps is between those at  $t = 0$  s and  $t = 15$  s since at  $t = 30$  s we are at the onset of an emission dominant process.

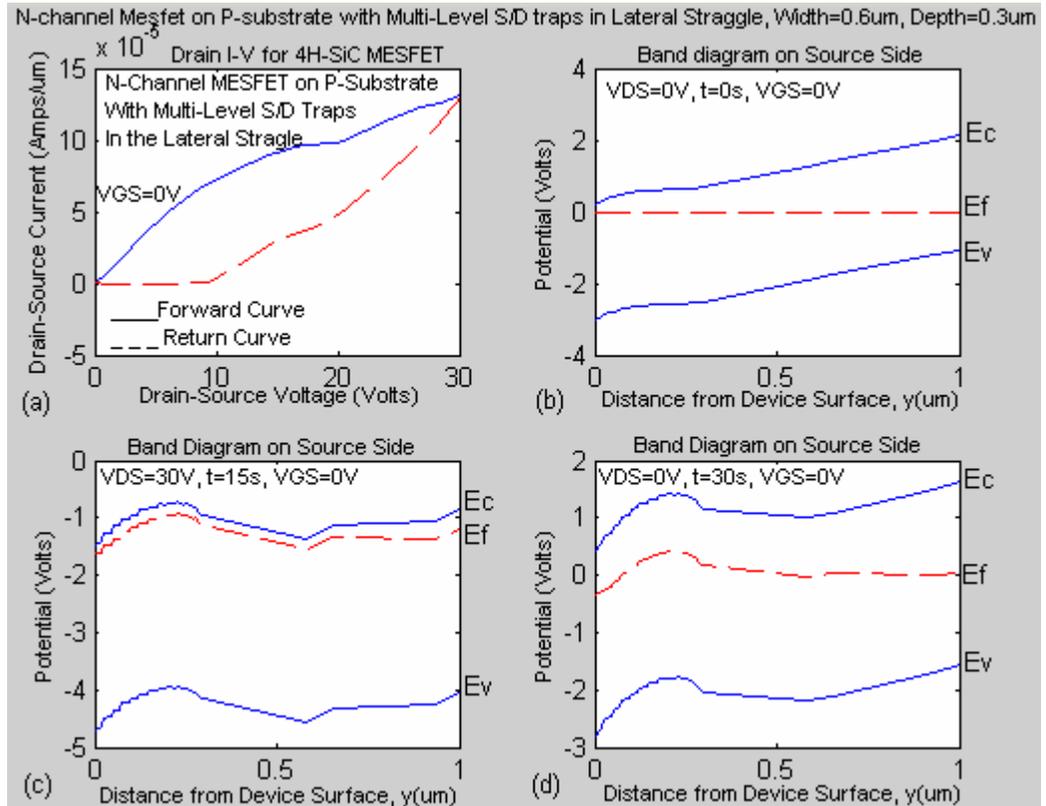


Figure A.26: (a) Simulated drain I-V curves at  $V_{GS} = 0 \text{ V}$  for 4H-SiC MESFET with multi-level traps representing source/drain residual implant damage traps in the lateral straggle (b) band diagram along trap region on source side at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$  (c) band diagram along trap region on source side at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$  (d) band diagram along trap region on source side at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ .

Figure A.28 also shows the corresponding electron densities long the trap regions on the source and drain sides. The figure indicates that at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$  the free electron density is the highest as suggested by the corresponding band diagram in Figure A.26. Thus electron capture is the dominant process at  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$  as already indicated, since for maximum capture to occur there has to be a high concentration of free electrons available to be captured. We also observe from Figure A.28 that the

concentration of free electrons is minimum at  $V_{DS} = 0$  V,  $t = 30$  s due to the excessive electron capture as  $V_{DS}$  falls back from  $V_{DS(max)}$  to 0 V. This is borne out by the corresponding band diagram at  $V_{DS} = 0$  V,  $t = 30$  s which shows a relatively high compensation of the material due to increased trapping of channel free electrons in the trap regions on both the source and drain sides. At  $V_{DS} = 0$  V,  $t = 0$  s the free electron density and the corresponding band diagram indicate that the material is less compensated than at  $V_{DS} = 0$  V,  $t = 30$  s due to the emission-dominant process at  $t = 0$  s. At  $t = 30$  s we are at the onset of the emission dominant process.

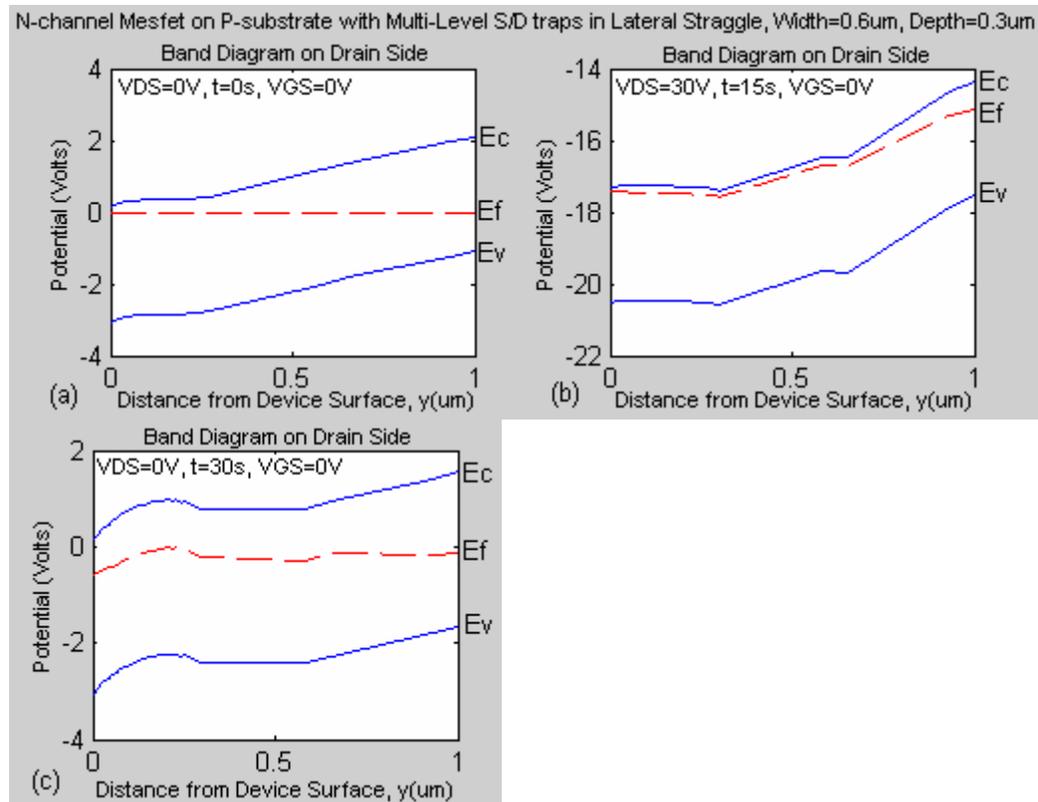


Figure A.27: Band diagram along trap region on drain side at (a)  $V_{DS} = 0$  V,  $t = 0$  s (b)  $V_{DS} = 30$  V,  $t = 15$  s (c)  $V_{DS} = 0$  V,  $t = 30$  s.

Figure A.29 depicts the band diagram at  $V_{DS} = 20$  V for the forward and return curves along the trap regions on the source and drain sides. The figure also depicts the corresponding trap occupation (empty trap density) and free electron concentration. We observe that due to trapping the band diagram shows more band bending in the channel area on the return curve than on the forward curve, particularly on the drain side. Correspondingly, the plots for trap occupation shows less empty trap centers for the return curve than for the forward curve, resulting in less free electron concentration on the return curve than on the forward curve.

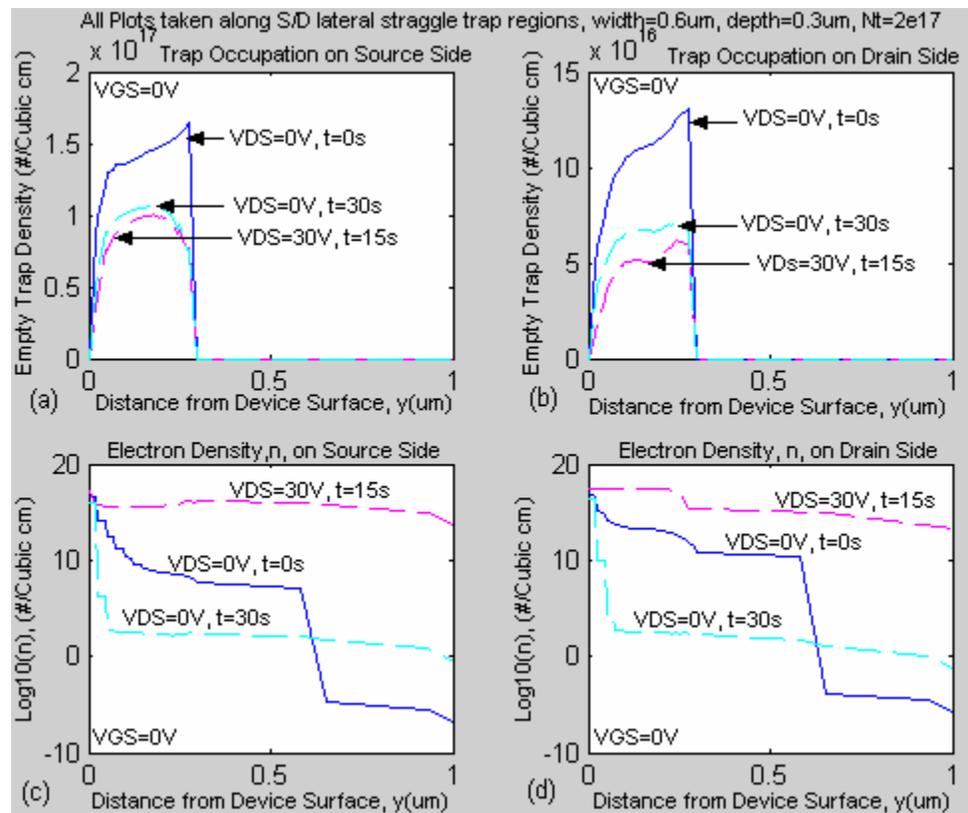


Figure A.28: Empty trap density at various  $V_{DS}$  and times along trap region at (a) source side (b) drain side, corresponding free electron density at (c) source side (d) at drain side.

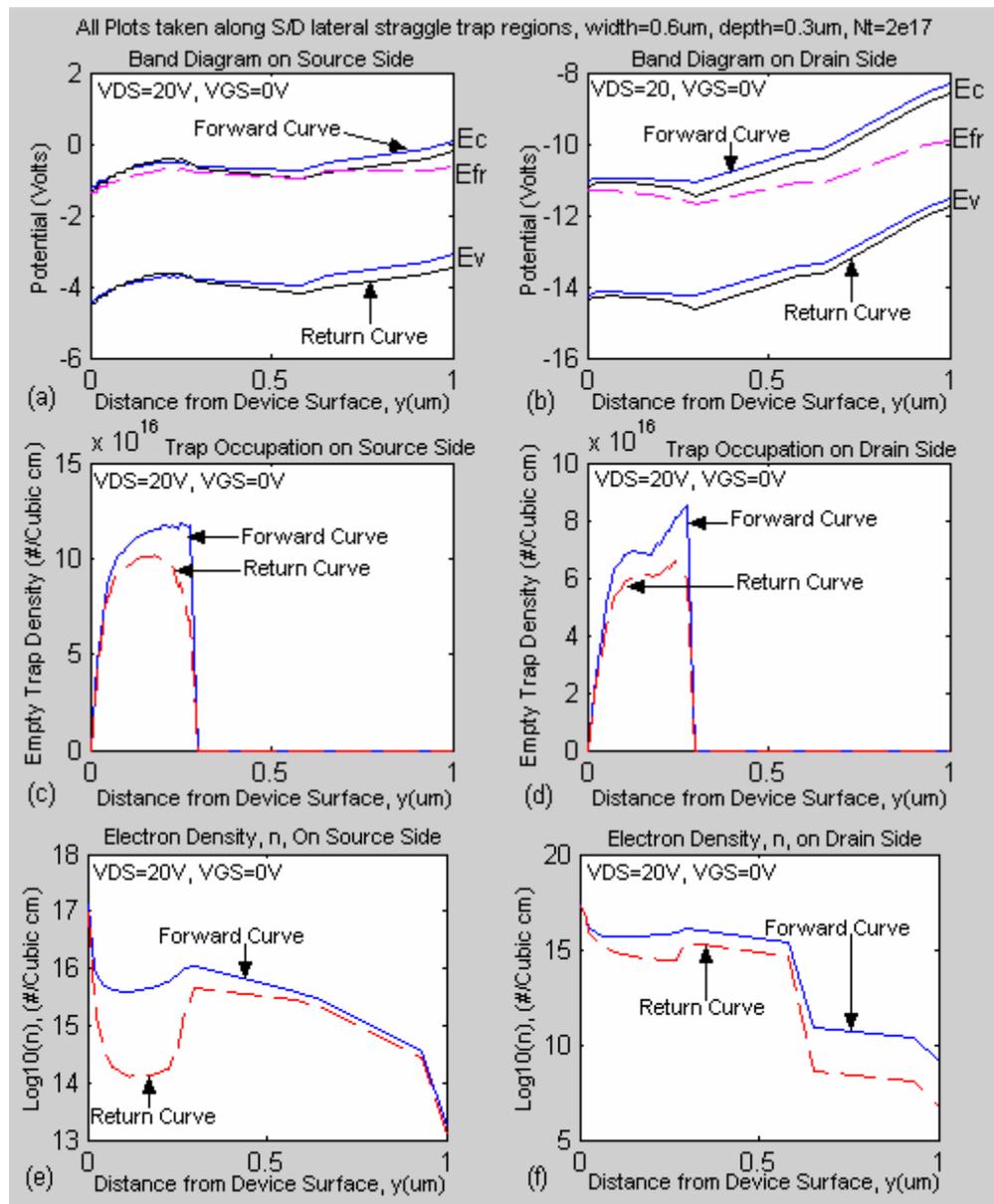


Figure A.29: Band diagram along trap region at  $V_{DS} = 20 \text{ V}$  for the forward and return curves at (a) source side (b) drain side, corresponding trap occupation at (c) source side (d) drain side, corresponding electron density at (e) source side (f) drain side.

In Figure A.30 the simulation is performed with a drain-source voltage rise-time of 0.01 s and fall-time of 29.99 s. It can be seen from the figure that due to the long fall-time of  $V_{DS}$  there will be more trapping of channel electrons leading to more band bending in the channel, particularly at the drain side as observed above. This suggests that much of the hysteresis in the drain I-V curves is due to the trapping and emission processes at the drain side because of the high electric fields at play at the drain region. It is the differences in the band diagrams, trap occupation and free electron density at a particular  $V_{DS}$  as  $V_{DS}$  rises and falls that lead to the hysteresis in the drain I-V characteristics.

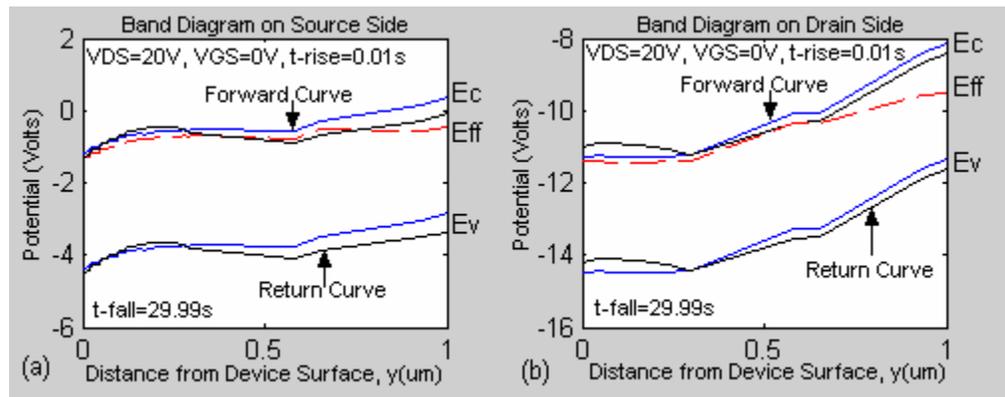


Figure A.30: Band diagram at  $V_{DS} = 20$  V for the forward and return curves for a rise-time of 0.01 s and fall-time of 29.99 s at (a) source side (b) drain side.

Using a single level trap with an energy level of 1.545 eV obtained by Dalibor et al. after  $\text{He}^+$ -implantation, the above simulation was repeated with trap concentration of  $1.8 \times 10^{17} \text{ cm}^{-3}$  and symmetric triangular pulse of 30 V amplitude and 30 s pulse width. Figure A.31 shows the drain I-V characteristics and the band diagrams along trap regions

on the source and drain sides at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$ ;  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$ ;  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ . Figure A.32 shows the corresponding trap occupation and electron density. The band diagrams on the source and drain sides show similar trends as in the multi-level case as  $V_{DS}$  rises and falls. A look at the source side band diagram indicates that at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$  the material is generally more compensated than at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$ . This is confirmed by the free electron density in Figure A.32, which shows the electron density at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$  to be generally greater than that at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$ . At the drain side, however, the band diagram at  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$  indicates the material to be more compensated than at  $t = 0 \text{ s}$  due to excessive trapping of channel electrons, which is borne out in Figure A.32 by the fact that the free electron density at  $t = 30 \text{ s}$  is less than that at  $t = 0 \text{ s}$ .

Figure A.33 shows the band diagrams at  $V_{DS} = 20 \text{ V}$  for the forward and return curves and the corresponding empty trap density and free electron concentration. As usual, the empty trap density on the return curves is less than that on the forward curves, indicating that more free electrons are trapped as  $V_{DS}$  falls from  $V_{DS(\max)} = 30 \text{ V}$  to  $0 \text{ V}$ . This is confirmed by the corresponding electron densities, which are lower on the return curves than on the forward curves. The band diagrams further show that there is more band bending on the return curve at the drain side than at the source side, suggesting that more trapping occurs at the drain side than at the source side as already mentioned elsewhere above. This is also borne out by the trap occupation plots and electron density plots, which show larger difference between the forward and return curves at the drain side than at the source side. The band diagram across the channel at a distance of  $0.1 \mu\text{m}$

from the device surface show that at  $t = 0$  s the potential barrier due to trapped electrons is about the same at the source and drain sides. At  $t = 30$  s, however, due to excessive electron trapping at the drain side as  $V_{DS}$  falls back to 0 V, the potential barrier at the drain side is higher than that at the source side. This indicates that much of the hysteresis in the drain I-V characteristics is due to trapping and emission processes at the drain side as a result of the high electric fields at the drain region as we have already mentioned.

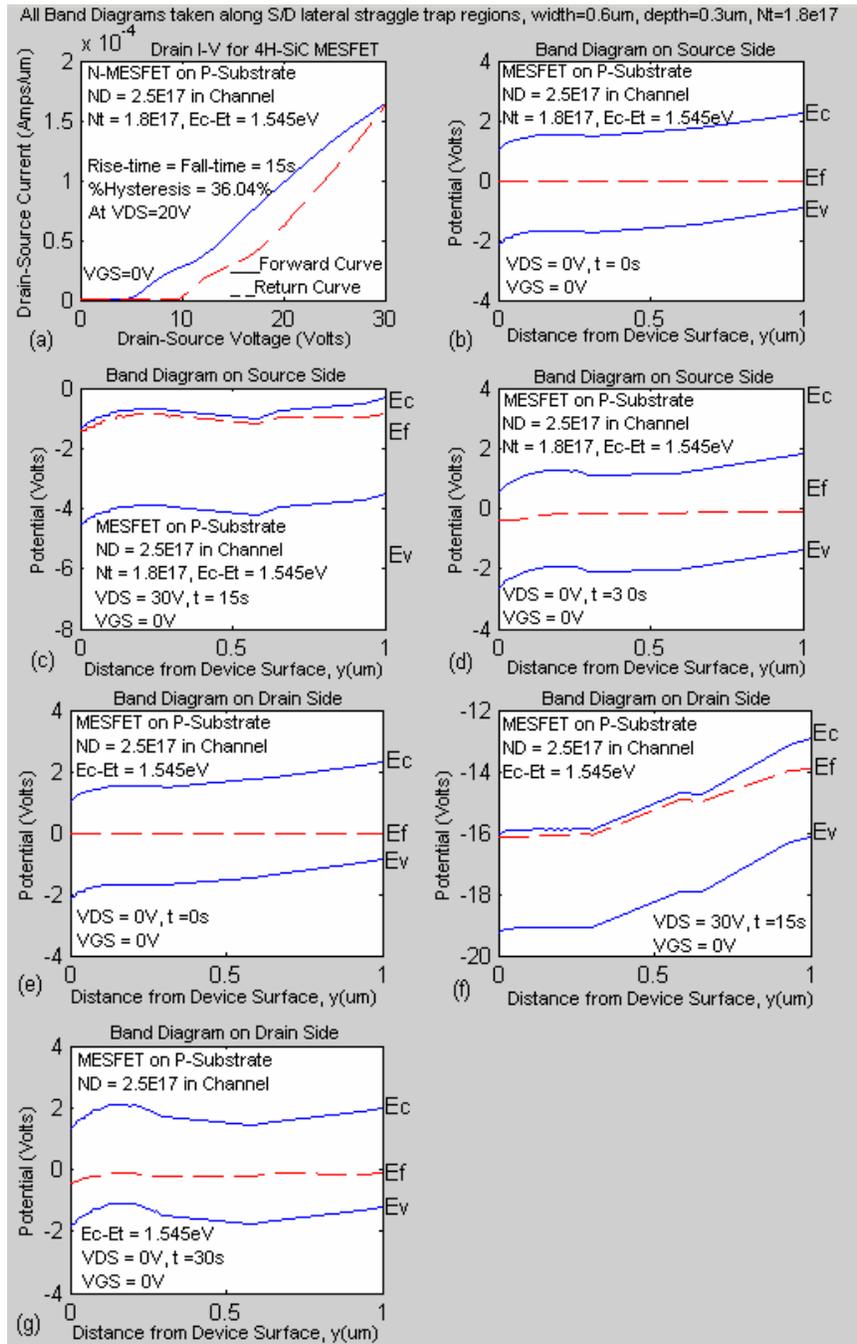


Figure A.31: (a) Simulated drain I-V curves for 4H-SiC MESFET at  $V_{GS}=0$  V. Band diagram at source side for (b)  $V_{DS} = 0$  V,  $t = 0$  s (c)  $V_{DS} = 30$  V,  $t = 15$  s (d)  $V_{DS} = 0$  V,  $t = 30$  s. Band diagram at drain side for (e)  $V_{DS} = 0$  V,  $t = 0$  s (f)  $V_{DS} = 30$  V,  $t = 15$  s (g)  $V_{DS} = 0$  V,  $t = 30$  s.

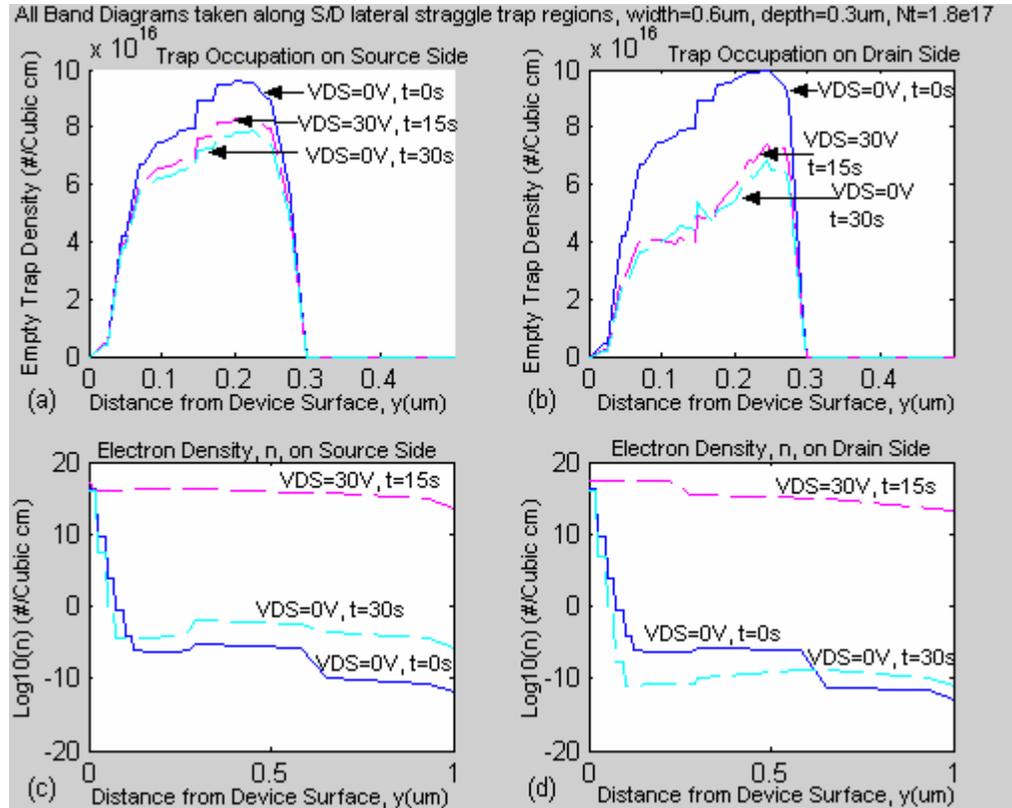


Figure A.32: Trap occupation at  $V_{DS} = 0 \text{ V}$ ,  $t = 0 \text{ s}$ ;  $V_{DS} = 30 \text{ V}$ ,  $t = 15 \text{ s}$ ;  $V_{DS} = 0 \text{ V}$ ,  $t = 30 \text{ s}$  at (a) source side (b) drain side, corresponding free electron density at (c) source side and (d) drain side.

Figure A.34 (a) and (b) show the simulated drain I-V characteristics for a 4H-SiC MESFET with channel traps representing source/drain residual implant damage lateral straggle traps at source only and drain only, respectively. We used a trap concentration of  $3.6 \times 10^{17} \text{ cm}^{-3}$  to obtain reasonable hysteresis and symmetric triangular pulse of 30 V amplitude and 30s for  $V_{DS}$ . We observe that with the traps at the source only the percent hysteresis at  $V_{DS} = 20 \text{ V}$  is only 15.59%, while with the traps at the drain only the percent hysteresis is 31.08%, which is twice the value with the traps at the source side only. This

confirms our observation that much of the hysteresis in the drain I-V curves in a device with channel traps is due to trapping and emission processes at the drain side.

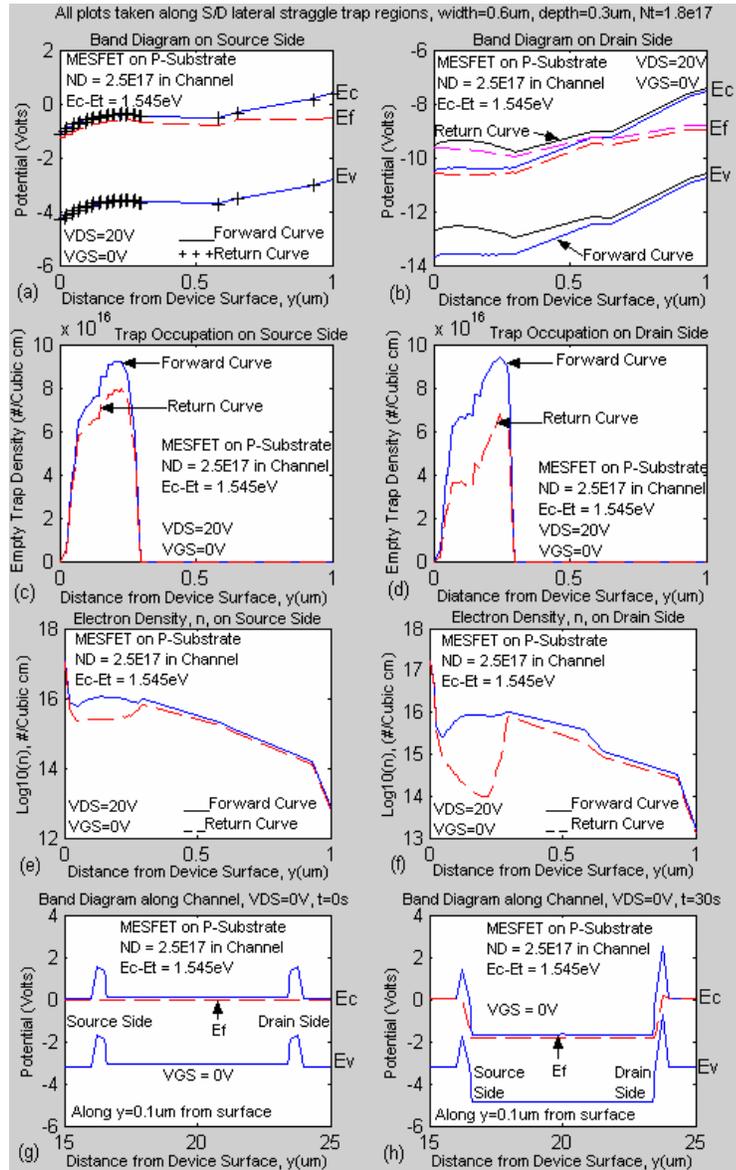


Figure A.33: Band diagram for 4H-SiC MESFET with single level trap at  $V_{DS} = 20$  V at (a) source side (b) drain side, corresponding trap occupation at (c) source side and (d) drain side. Free electron density at (e) source side (d) drain side. Band diagram along channel at (g)  $V_{DS} = 0$  V,  $t = 0$  s (h)  $V_{DS} = 0$  V,  $t = 30$  s.

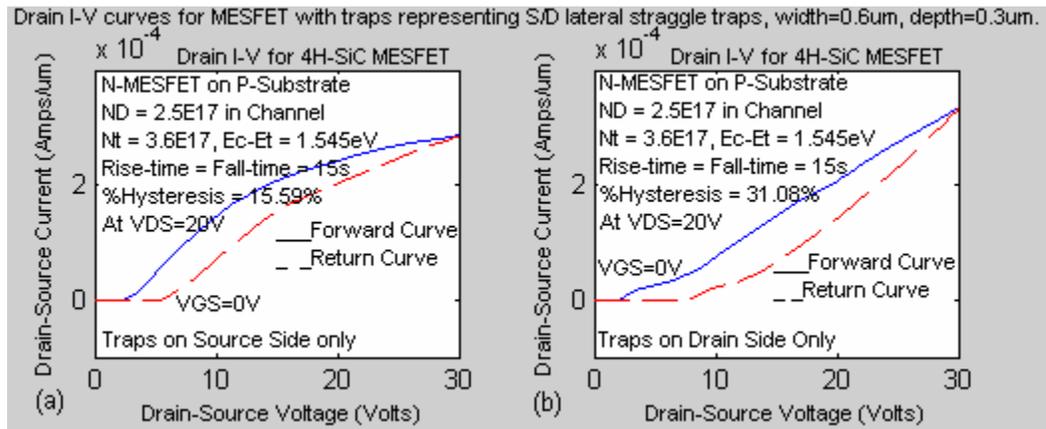


Figure A.34: Simulated drain I-V curves for 4H-SiC MESFET with traps representing source/drain residual implant lateral straggle traps at (a) the source side only and (b) the drain side only.

### A.3 MESFET with Substrate Traps only – with p-Buffer Layer

The mechanism for the hysteresis (looping) in the drain I-V characteristics of MESFET with p-buffer layer is basically similar to that without p-buffer layer. However, in the case of a device with p-buffer layer, the hysteresis is due to the presence of deep level electron traps on the substrate side of the buffer-substrate interface. At high  $V_{DS}$  the buffer layer-active layer p-n junction becomes highly reverse biased. As a result, the p-buffer layer can be fully depleted, and because of the high electric, electrons can be injected from the channel into the substrate where they may be trapped [14]. This results in a negatively charged depleted space charge region on the substrate side of the buffer-substrate interface, which induces a symmetrical depleted positive space charge region at the lower portion of the channel [14], constricting the channel and reducing the drain current in the process. As in the case of the device without p-buffer, the negative space

charge on the substrate side of the buffer-substrate interface act as a parasitic backgate, which leads to drain current reduction or drain current collapse [14].  $V_{DS}$  modulates the negative space charge (backgate) on the substrate side of the buffer-substrate interface as it rises and falls, depending on the quantity of trapped electrons. This in turn modulates the induced symmetric depleted positive space charge as  $V_{DS}$  rises and falls, leading to the hysteresis in the drain I-V characteristics.

Figure A.35 shows the simulated drain I-V characteristics at  $V_{GS} = -20$  V of MESFET with p-buffer layer and substrate traps only and Figure A.36 shows the band diagram under the gate (along the center of the gate) at  $V_{DS}=19$  V for the forward and return curves. Figure A.36b shows the expanded view of the band diagram. As in the case for the device without p-buffer layer, the band diagrams suggest that capture is the dominant process as  $V_{DS}$  falls and emission is the dominant process as  $V_{DS}$  rises. Due to the captured electrons the interface potential barrier (conduction band edge) is higher for the return curve ( $V_{DS}$  falling) than it is for the forward curve ( $V_{DS}$  rising) where electron emission from trap centers is the dominant process, in accordance with the Poisson law, as already pointed out. The band diagram for the return curve further show that electron capture begins in the buffer with shallow acceptors and increases into the substrate with the deep level acceptors there, leading to increased potential barrier height as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V. In addition the band diagram (return curve) shows that, the buffer layer is completely depleted.

Comparing Figure A.35 to Figure A.2, which is the drain I-V characteristics at  $V_{GS} = -20$  V for MESFET with substrate traps only and without p-buffer layer, we see

drastic reduction in the looping (hysteresis) in the drain I-V curve for the device with p-buffer layer for the same trap parameters. Comparing the band diagrams in Figures A.3 and A.36, we see that there is little or no potential barrier at the substrate side of the channel-substrate interface for the forward curve ( $V_{DS}$  rising) for the device without p-buffer relative to the potential barrier at buffer side of the channel-buffer interface for the device with p-buffer. The device with p-buffer has higher potential barrier at buffer side of the channel-buffer interface for the forward curve due to the presence of the lightly doped p-buffer layer.

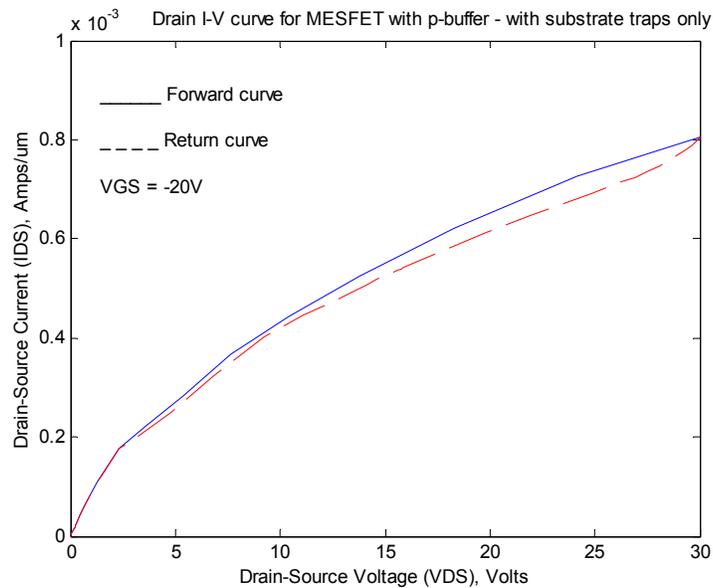
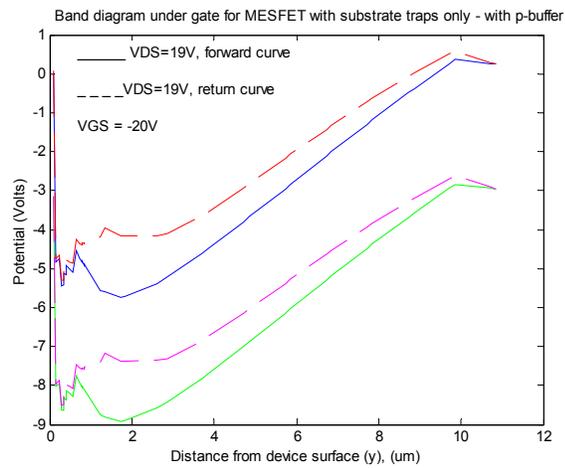


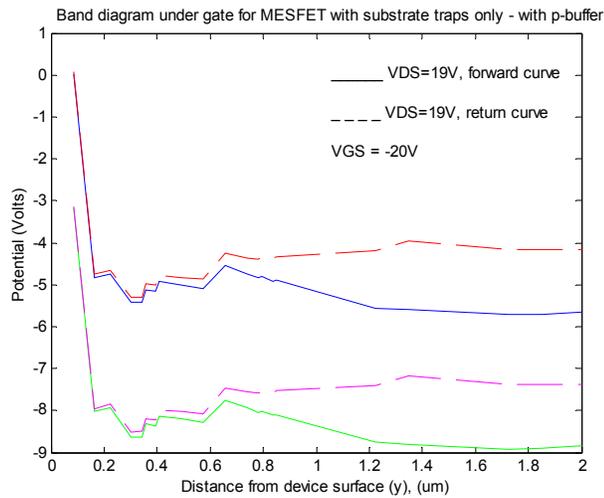
Figure A.35: Simulated drain I-V characteristics for MESFET with p-buffer layer and substrate traps only.

This leads to less trapping of channel electrons during the capture-dominant phase as  $V_{DS}$  falls from  $V_{DS(\text{max})} = 30 \text{ V}$  to 0 V. Thus for both the forward and return curves, there is less emission and trapping of channel electrons compared to the device without p-

buffer as shown in the 3-D trap occupation plots in Figure A.37 and Figure A.7. Consequently, for a given  $V_{DS}$ , there is less difference between the forward current and return current for the device with p-buffer than for the device without p-buffer, leading to less looping in the drain I-V characteristics for the former.

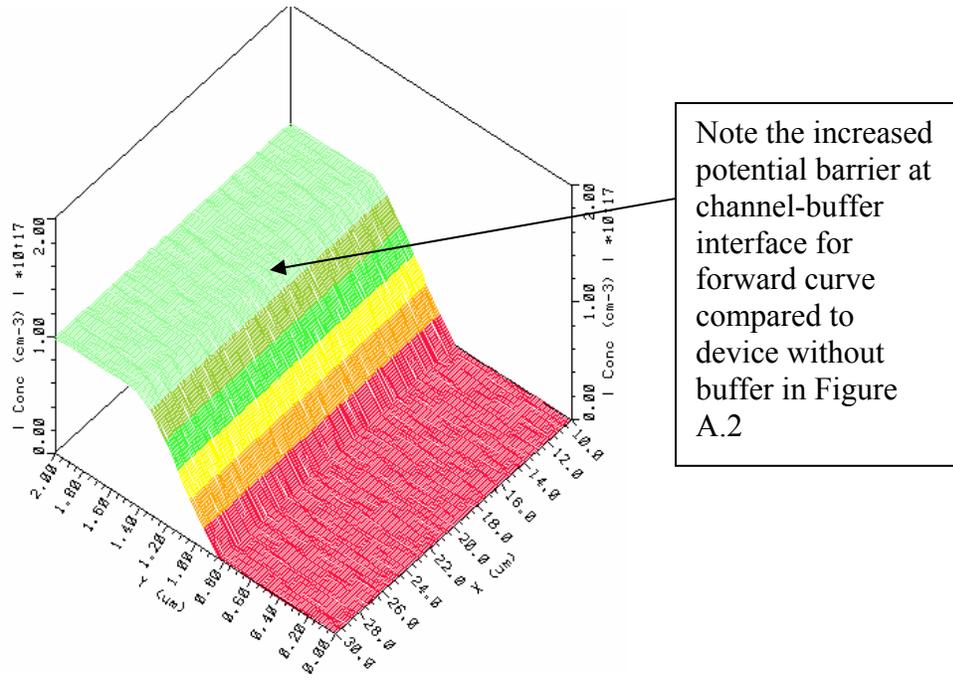


(a)

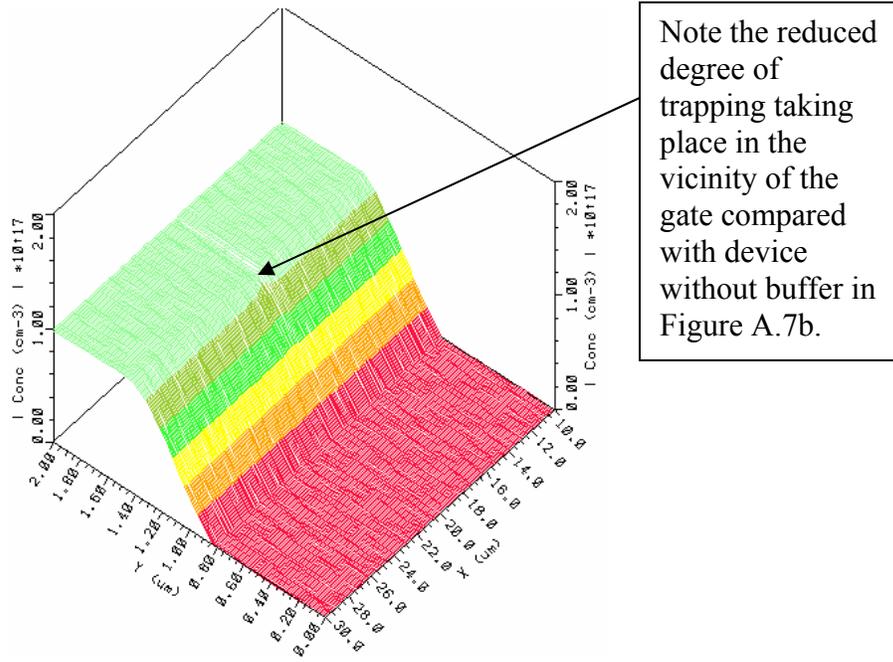


(b)

Figure A.36: (a) Band diagram under gate for MESFET with p-buffer layer and substrate traps only (b) expanded view.



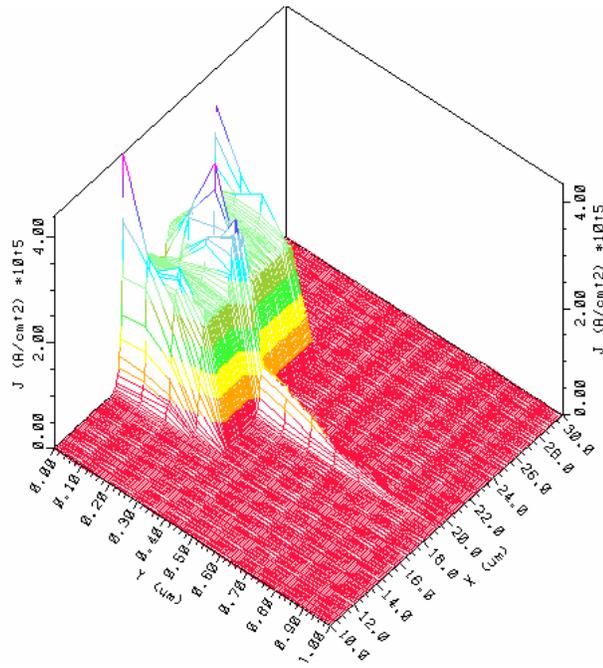
(a)



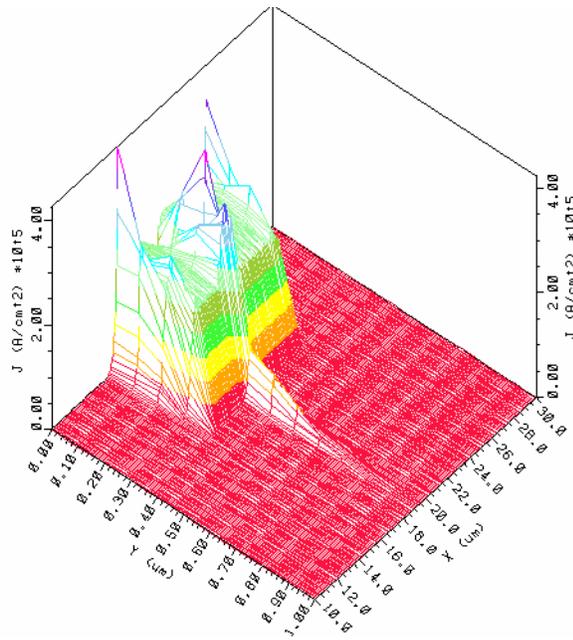
(a)

Figure A.37: 3-D trap occupation (empty, unoccupied trap centers) for MESFET with p-buffer layer and substrate traps only at (a)  $V_{DS} = 19$  V forward curve and (b)  $V_{DS} = 19$  V return curve.

This is borne out by the subtle difference between the 3-D current distribution for the forward and return curves at  $V_{DS} = 19V$  shown in Figure 5.29. This is in contrast to the relatively large difference in the 3-D current distribution at  $V_{DS} = 19 V$  between the forward and return curves for the device without p-buffer as shown in Figure A.10. Thus for the MESFET with p-buffer layer, the presence of greater potential barrier at the buffer side of the channel-buffer interface leads to reduced trapping of channel electrons as  $V_{DS}$  falls from  $V_{DS(max)}$  to 0 V and therefore reduced emission and trapping processes as  $V_{DS}$  rises and falls leading to decreased hysteresis in the drain I-V characteristics. Thus the processes that lead to hysteresis in the drain I-V characteristics for MESFET with p-buffer layer are similar to those for the device without p-buffer layer but on a smaller scale due to the presence of the additional potential barrier due to the p-buffer layer.



(a)



(b)

Figure A.38: 3-D current distribution for MESFET with p-buffer layer and substrate traps only at  $V_{DS} = 19$  V on (a) the forward curve (b) the return curve.

## APPENDIX B

### SUBTLE EFFECTS OF SOURCE/DRAIN IMPLANT DAMAGE TRAPS – SIMULATION APPROACH

## APPENDIX B

### Subtle Effects of Source/Drain Implant Damage Traps – Simulation Approach

In this section, Medici will be used to investigate a number of subtle effects of traps resulting residual implant lattice damage traps on MESFET drain-source current. For these simulation investigations, the simulation MESFET devices will be constructed on conductive p-type substrates with only source/drain residual implant damage traps and no substrate traps. This allows only the effects of the residual implant lattice damage traps to be studied.

#### B.1 Substrate Currents with and without Residual Implant Damage Traps

Figure B.1 shows the two-dimensional current contours of a simulation MESFET on p-type conductive substrate without source/drain residual implant damage traps and Figure B.2 shows the current contours of the simulation device with source/drain implant damage traps all at  $V_{GS} = 0$  V and  $V_{DS} = V_{DS(max)} = 15$  V also on p-type substrate without any substrate traps. We observe from these figures that, there is more substrate currents in the simulation device without source/drain implant damage traps than in the simulation device with implant damage traps. Thus the residual implant damage traps reduce the substrate currents.

Mesfet on p-substrate: Current Contours, VGS=0V, VDS<max>=15V

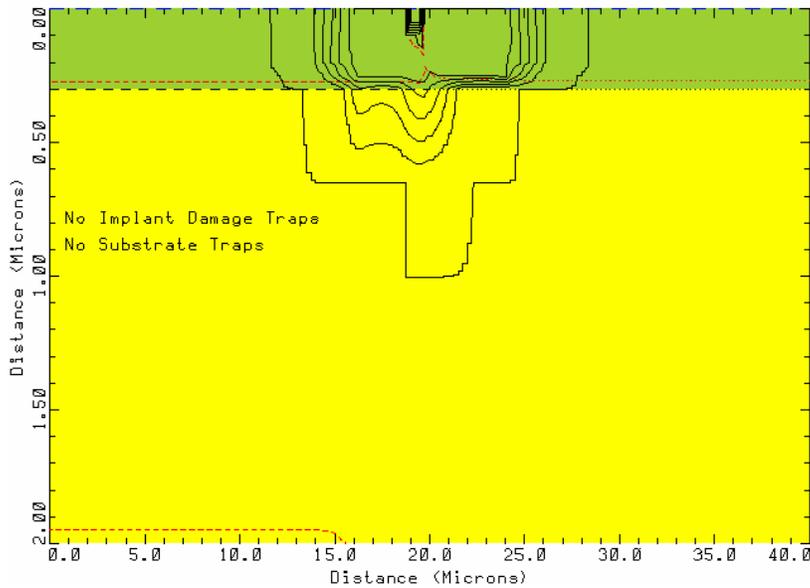


Figure B.1: Two-Dimensional current contours of simulation MESFET on p-type substrate without source/drain residual implant lattice damage traps.

Mesfet on p-substrate: Current Contours, VGS=0V, VDS<max>=15V

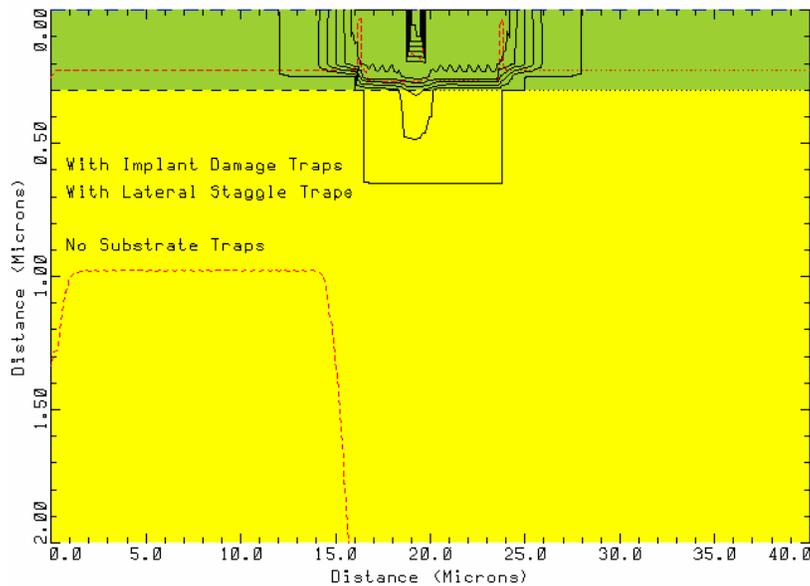


Figure B.2: Two-Dimensional current contours of simulation MESFET on p-type substrate with source/drain residual implant lattice damage traps. Note the reduction in substrate current.

Figure B.3 shows the drain I-V characteristics of a simulation MESFET with residual source/drain implant damage traps and Figure B.4 shows the drain I-V characteristics for the same device without source/drain residual implant damage traps. We observe that without the source/drain residual implant damage traps hysteresis does not appear in the I-V curves. We further note from Figure B.4 that, due to the absence of the source/drain residual implant damage traps, the current levels are relatively higher than in Figure B.3 in which source/drain residual implant damage traps are present. Hence, the source/drain residual implant lattice damage traps introduce some channel resistance that tends to reduce the drain-source current levels and also reduces the substrate currents as seen in Figure B.2.

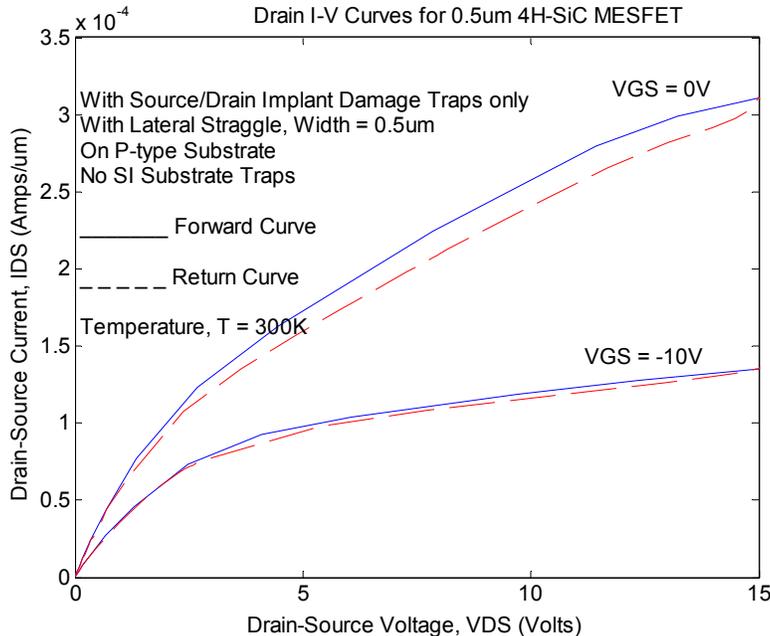


Figure B.3: Drain I-V curves for simulation MESFET with source/drain residual implant lattice damage traps.

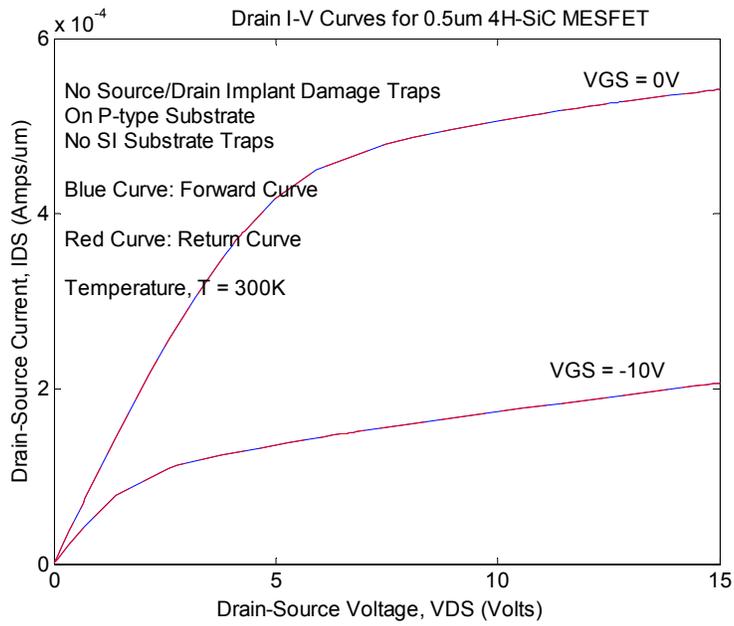
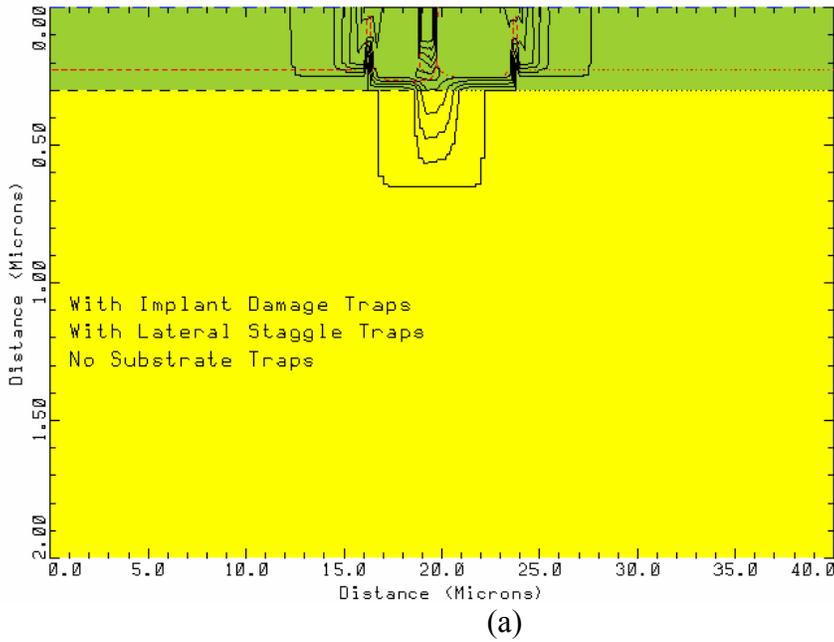


Figure B.4: Drain I-V characteristics of a simulation MESFET without source/drain residual implant lattice damage traps.

MESFET on P-substrate: Current Contours,  $V_{GS}=-10V$ ,  $V_{DS(max)}=15V$



MESFET on P-substrate: Current Contours,  $V_{GS}=-10V$ ,  $V_{DS(max)}=15V$

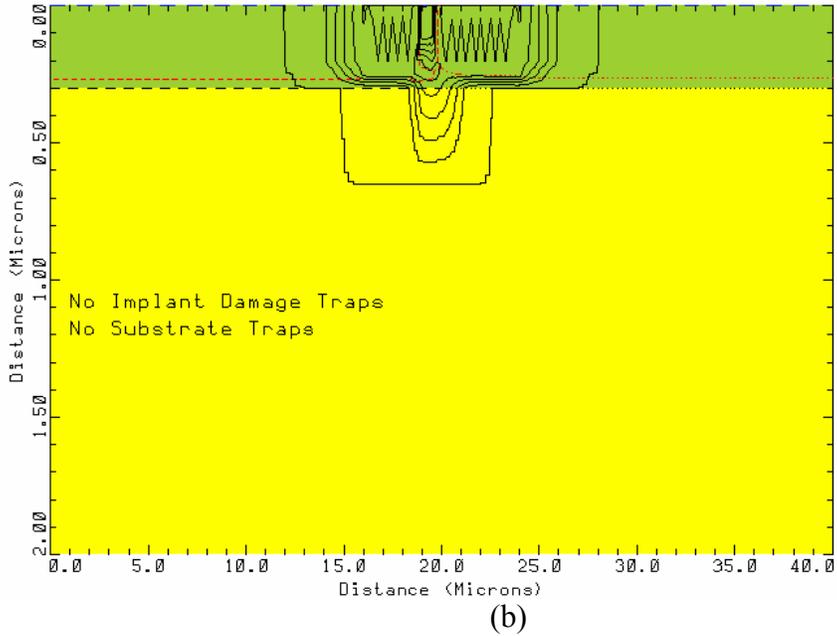
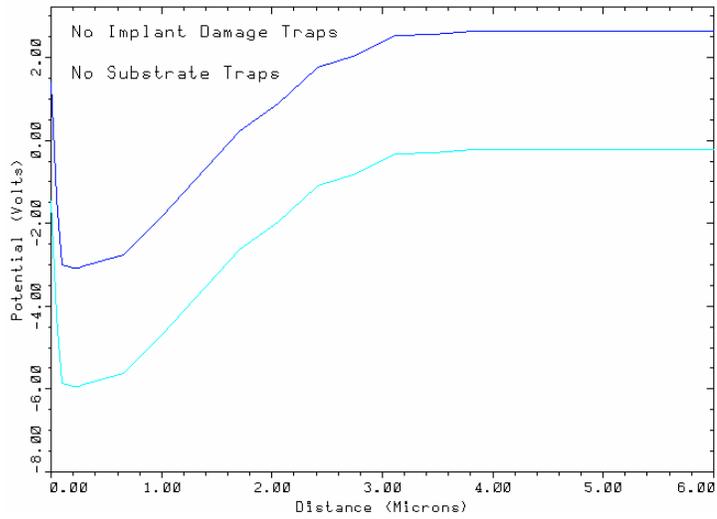


Figure B.5: Two-Dimensional Current Contours for simulation MESFET for  $V_{GS} = -10 V$   
(a) with source/drain residual implant lattice damage traps (b) without source/drain residual implant lattice damage traps.

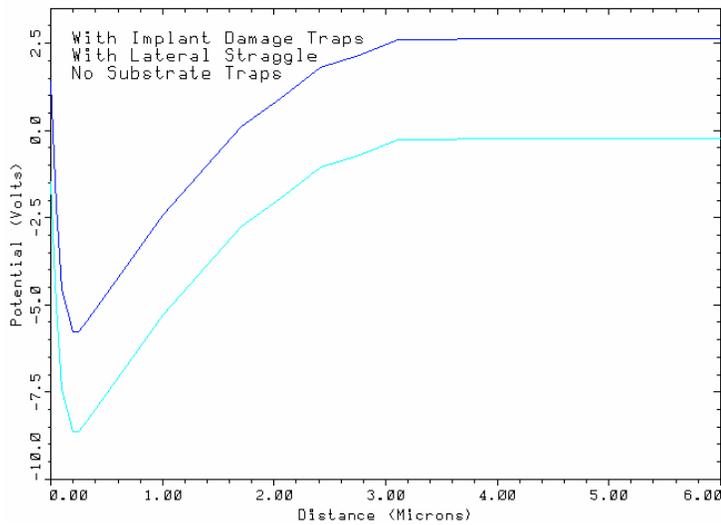
For high negative  $V_{GS}$  such as  $V_{GS} = -10$  V, however, the depth of substrate currents is the same for both the device with and the device without source/drain residual implant lattice damage traps, although the substrate current is a little more spread out for the device without implant damage traps as shown in Figure B.5 above. This is because at high  $V_{GS}$  the potential barrier at the channel-substrate interface is higher than that at  $V_{GS} = 0$  V reducing the number of electrons injected into the substrate from the channel, and hence reducing the depth of the substrate current. Figures B.6 and B.7 show the band diagram at  $V_{GS} = 0$  V and  $V_{GS} = -10$  V respectively for simulation MESFETs with and without source/drain residual implant lattice damage traps. It is worth noting that, the interface potential barrier in the device with implant damage traps at  $V_{GS} = 0$  V is higher ( $\sim 8.5$  V) than in the device without implant damage traps ( $\sim 5.5$  V) also at  $V_{GS} = 0$  V. This further helps to explain why there is reduced substrate current in the former. Figures B.7 (a) and (b) show that the interface potential barrier is the same for both the devices with and without source/drain implant damage traps, explaining why the depth of the substrate current is the same for the two types of simulation devices.

MESFET on P-substrate: Band Diagram under Gate,  $V_{GS}=0V$ ,  $V_{DS}=15V$



(a)

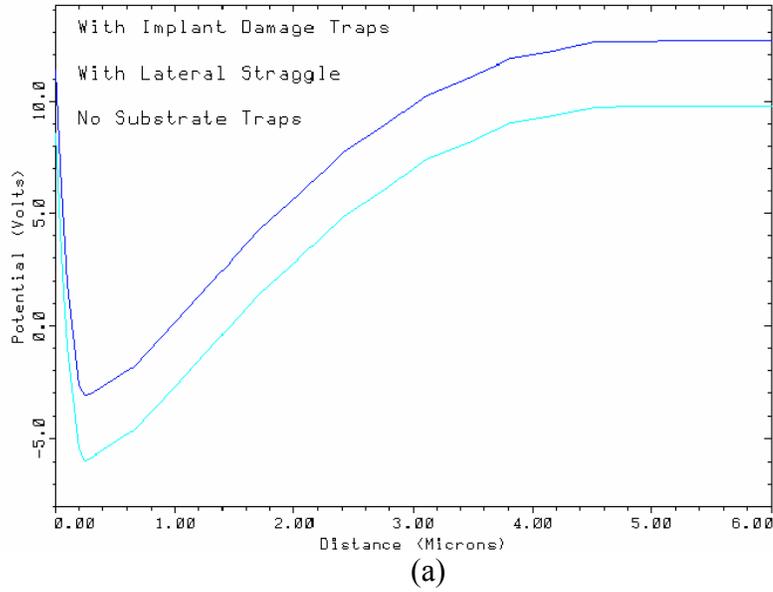
MESFET on P-substrate: Band Diagram under Gate,  $V_{GS}=0V$ ,  $V_{DS}=15V$



(b)

Figure B.6: Band diagram under gate for simulation device at  $V_{GS} = 0 V$  (a) without and (b) with source/drain residual implant lattice damage traps.

MESFET on P-substrate: Band Diagram under Gate,  $V_{GS}=-10V$ ,  $V_{DS}=15$



MESFET on P-substrate: Band Diagram under Gate,  $V_{GS}=-10V$ ,  $V_{DS}=15V$

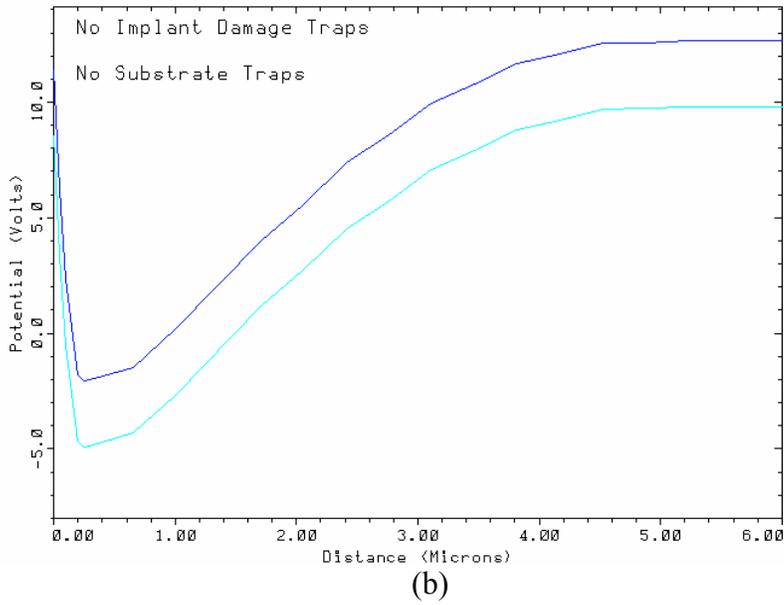


Figure B.7: Band diagram under gate for simulation device at  $V_{GS} = -10 V$  (c) with source/drain residual implant lattice damage traps (d) without source/drain residual implant lattice damage traps.

## **B.2 Effects of Lateral Straggle on Drain I-V Curves and Substrate Currents**

Figure B.8 exhibits the drain I-V characteristics of a simulation MESFET with source/drain residual implant lattice damage traps but without traps due to lateral straggle. It can be seen that without the lateral straggle traps, no hysteresis is observed in the drain I-V curves, as compared to I-V characteristics of the simulation device in Figure B.3 in which traps due to lateral straggle are present. It is interesting to observe that the drain I-V curves in Figure B.8 are similar to those in Figure B.4 for a simulation device with no source/drain implant damage traps. Furthermore, the current levels are the same. It can therefore be inferred that, it is the traps due to the lateral straggle of residual source/drain implant lattice damage, that control the current levels and the hysteresis in the drain I-V curves. In addition, if we compare the two-dimensional current contours for the simulation device with source/drain implant damage traps but no traps due to lateral straggle in Figure B.9 to those in Figure B.1 for the device without source/drain residual implant lattice damage traps, we observe that the depth of the two contour plots are the same, although the substrate current in Figure B.1 is a little more spread out. This further suggests that it is the traps due to the lateral straggle that controls the behavior of the drain-source currents. This is due to the fact that the drain-source current largely flows between the inside edges of the source and drain in the channel area as can be observed in the two-dimensional current contour plots in Figures B.1, B.2, B.5, and B.9.

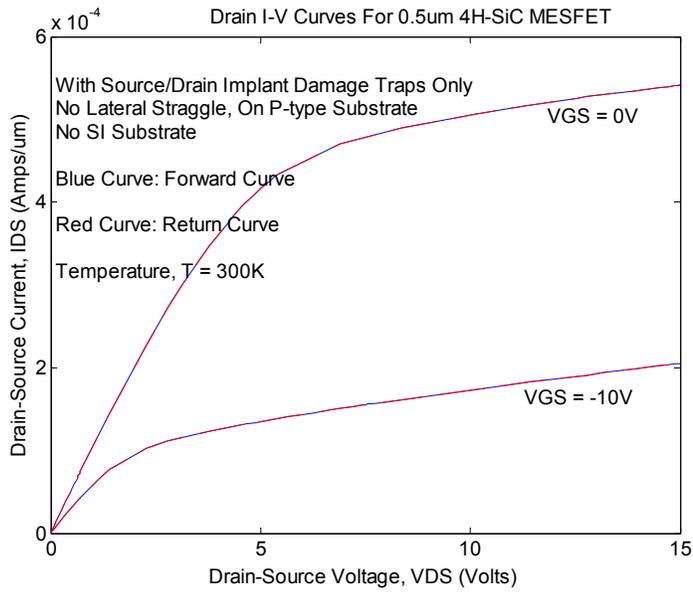


Figure B.8: Drain I-V characteristics of a simulation MESFET on p-type substrate with source/drain residual implant lattice damage traps but no traps due to lateral straggle.

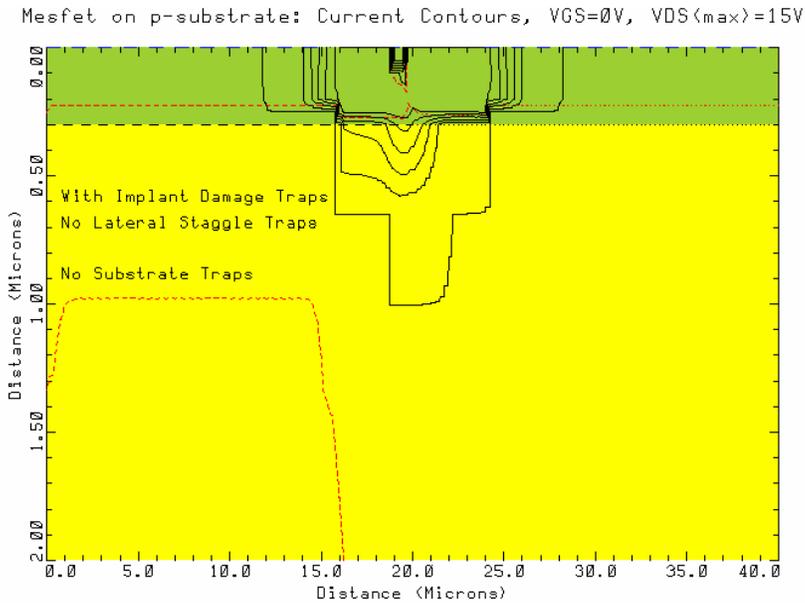


Figure B.9: Two-dimensional current contours for simulation MESFET on p-type substrate with source/drain residual implant lattice damage traps but no traps due to lateral straggle.

### B.3 Effects of Lateral Straggle Width on Drain I-V Characteristics and Substrate Currents

In this section we investigate the effects of the width of the traps used to represent lateral straggle implant damage traps on the drain I-V characteristics and substrate currents. The drain I-V curves and the substrate currents are calculated (simulated) for various widths of the lateral straggle. From Figures B.4, B.8, and B.10 we observe that the drain I-V curves for the simulation MESFETs with no source/drain residual implant damage traps, with source/drain residual implant damage traps but no lateral straggle, and with source/drain residual implant damage traps with lateral straggle width of  $0.2 \mu\text{m}$  respectively are similar. All three set of I-V characteristics have no hysteresis and they all have the same current levels.

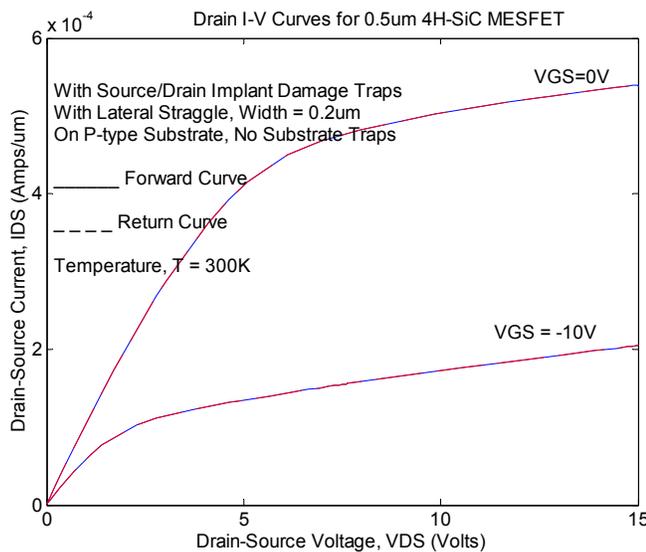
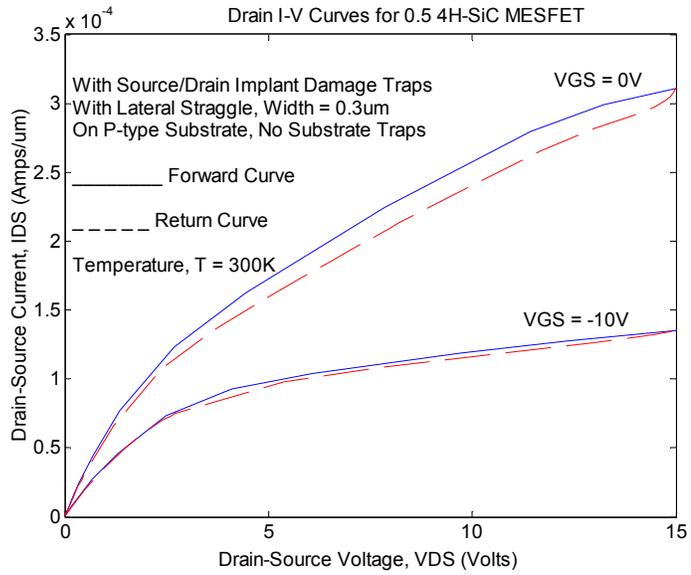
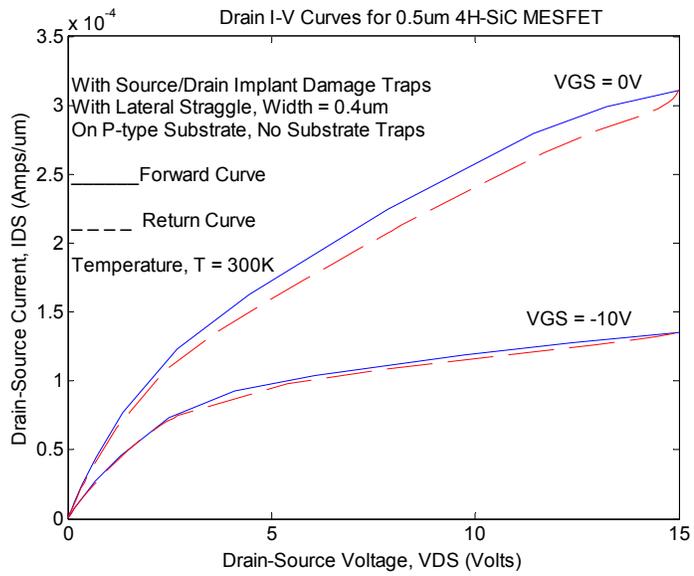


Figure B.10: Drain I-V characteristics of simulation MESFET with lateral straggle Width =  $0.2 \mu\text{m}$ .

As the width of the lateral straggle increases from 0.2  $\mu\text{m}$  to 0.3  $\mu\text{m}$  and beyond hysteresis appear in the I-V curves. We further observe from Figures B.11 and B.12 that at lateral straggle widths of 0.3  $\mu\text{m}$ , 0.4  $\mu\text{m}$ , and 0.5  $\mu\text{m}$  the degree of hysteresis and current levels are the same. Between 0.5  $\mu\text{m}$  and 0.6  $\mu\text{m}$  of lateral straggle width, the hysteresis and current levels begin to decrease and continue to decrease as the lateral straggle width increases beyond 0.6  $\mu\text{m}$ .



(a)



(b)

Figure B.11: Drain I-V characteristics of simulation MESFETs with varying lateral straggle width. (a) Lateral straggle width = 0.3  $\mu\text{m}$  (b) Lateral straggle width = 0.4  $\mu\text{m}$ .

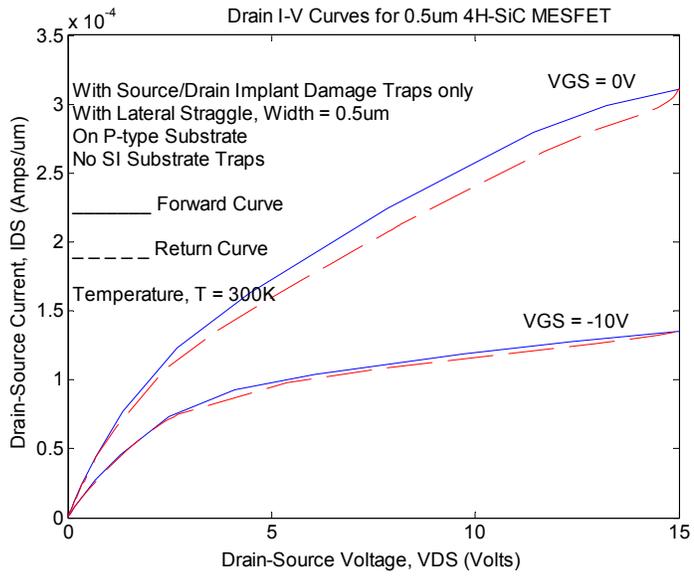


Figure B.12: Drain I-V characteristics of simulation MESFETs with lateral straggle width = 0.5  $\mu\text{m}$ .

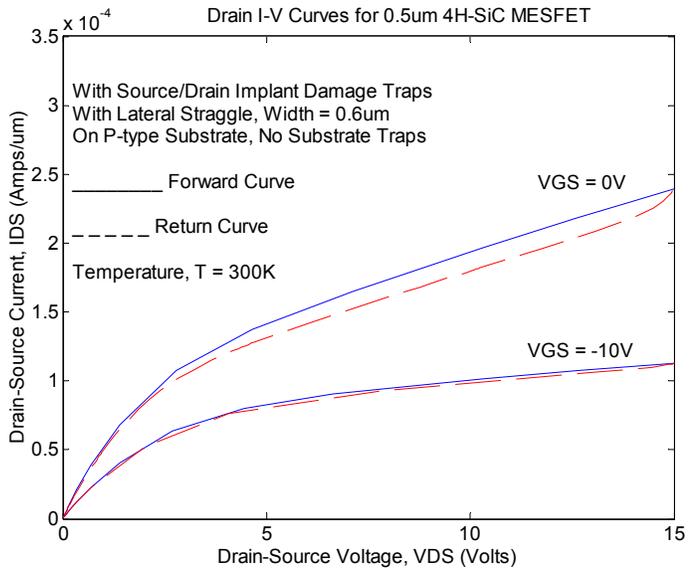
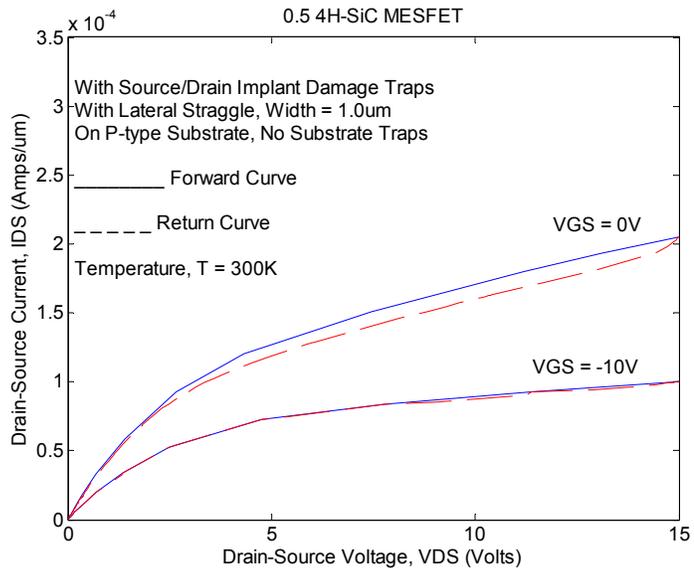
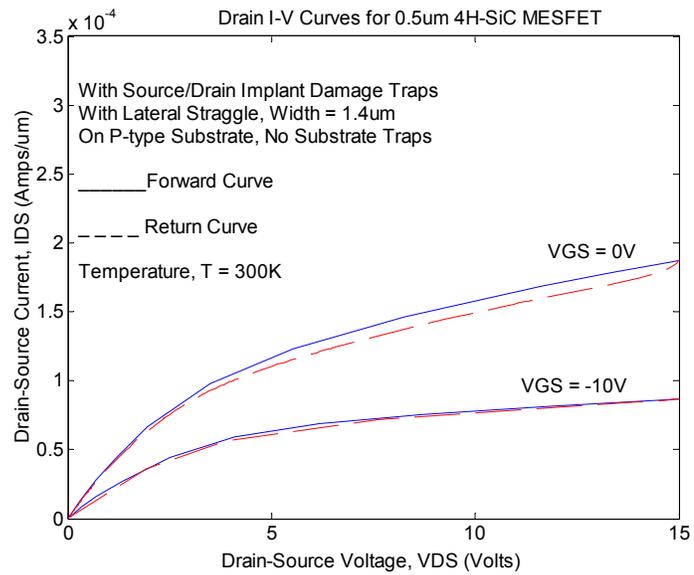


Figure B.13: Drain I-V Curves for simulation MESFET with lateral straggle width = 0.6  $\mu\text{m}$ .

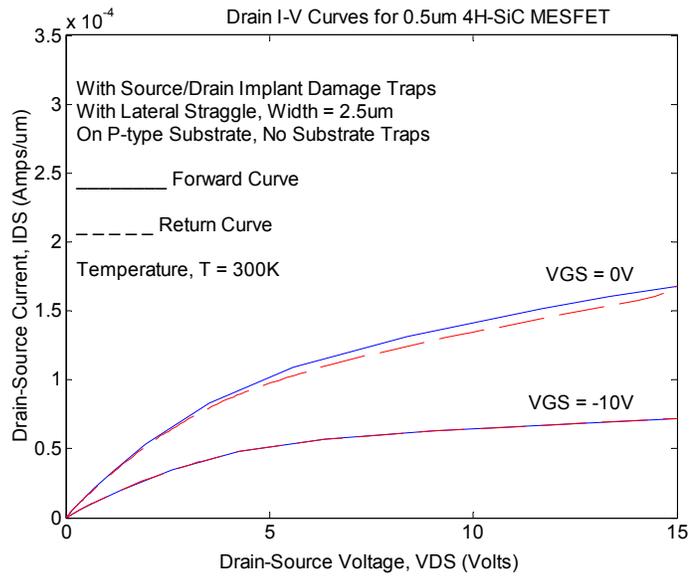


(a)

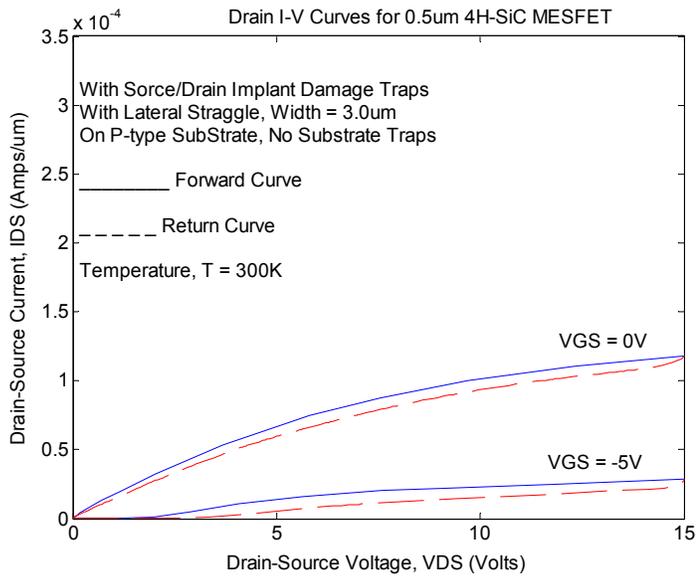


(b)

Figure B.14: Drain I-V curves for simulation MESFET with (a) lateral straggle width = 1.0  $\mu\text{m}$  (b) lateral straggle width = 1.4  $\mu\text{m}$ .



(a)

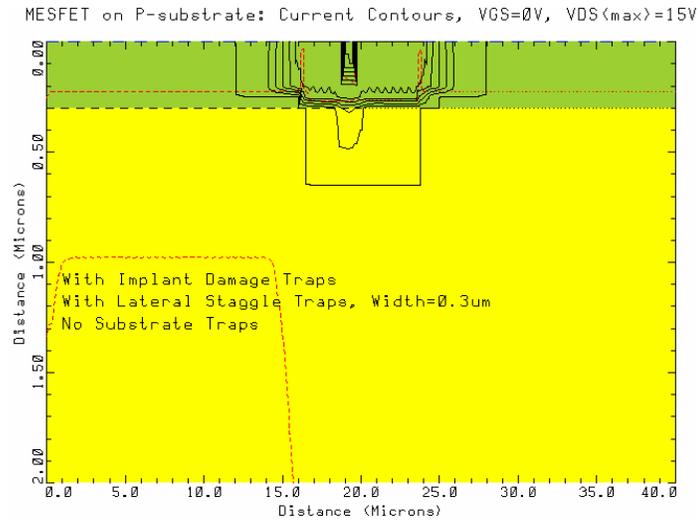


(b)

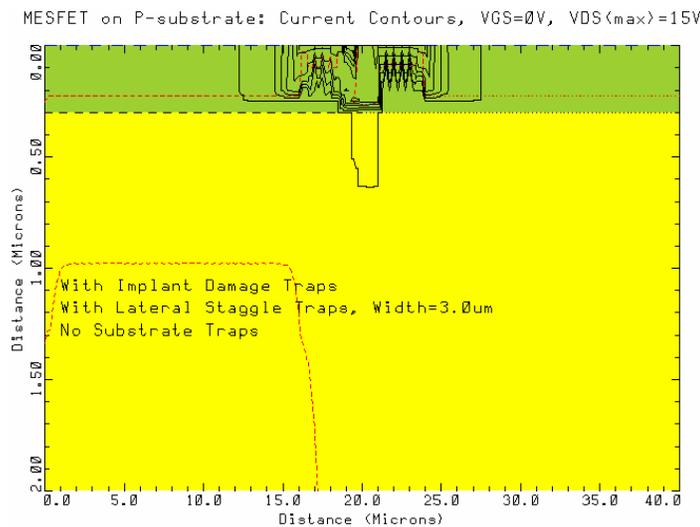
Figure B.15: Drain I-V curves for simulation MESFET with (a) lateral straggle width = 2.5  $\mu\text{m}$  (b) lateral straggle width = 3.0  $\mu\text{m}$ .

The above trend can be explained as follows. As the width of the lateral straggle increases, there is a corresponding increase in the concentration of traps due to lateral straggle, which are introduced into the channel. This reduces the free electron concentration in the channel and hence the drain-source current levels due to the trapping of channel electrons. Since the degree of hysteresis directly depends on the concentration of free electrons available to be trapped, the degree of hysteresis decreases as the width of the lateral straggle increases since increased lateral straggle width introduces more traps into the channel. The increased channel traps, brought about by increasing lateral straggle width, also has the effect of increasing the channel resistance due to trapping of channel free electrons. This reduces the channel drain-source current and therefore the hysteresis in the I-V curves, since there are fewer electrons involved in current conduction and to be trapped. Furthermore, we can see from above figures that as the lateral straggle width increases the pinch-off voltage decreases due to decreased channel free electron concentration. This can be particularly observed by comparing Figures B.11 to B.15. Ordinarily pinch-off is due to the depletion of the channel of free electrons under the gate and/or drain by the increasing applied gate and drain voltages, leading to  $I_{DS} = 0$  A at  $V_{GS} = V_{pinch-off}$ . It seems that the traps introduced into channel by increasing lateral straggle depletes the channel of free electrons by trapping channel electrons and creates an effect similar to increasing  $V_{GS}$  and/or  $V_{DS}$ . In addition, as lateral straggle width increases substrate currents decreases. This is due to decreased free electron concentration in the channel brought about by increased trapping of channel electrons by the increasing number of lateral straggle traps introduced by the increasing lateral straggle width. Hence

fewer channel electrons are injected into the substrate, leading to reduced substrate current with increasing lateral straggle width as shown in Figure B.16 below. As already noted, it is the traps due to lateral straggle that controls the magnitude of hysteresis and current levels.



(a)



(b)

Figure B.16: Current contours for simulation MESFET with (a) lateral straggle width =  $0.3 \mu\text{m}$  and (b) lateral straggle width =  $3.0 \mu\text{m}$ .

#### **B.4 Effect of the Depth of Implant Damage Traps on Drain I-V Characteristics**

In this section, the effects of the depth of implant damage traps on drain I-V characteristics will be investigated. With a lateral straggle width of  $0.5\ \mu\text{m}$ , no hysteresis appear in the drain I-V curves for source/drain implant damage traps depth less than  $0.3\ \mu\text{m}$  as can be observed from Figures B.17 and B.18(a). However, as can be seen from Figure B.18b, hysteresis begins to appear in the drain I-V characteristics when the implant damage traps depth is  $3.0\ \mu\text{m}$ , which is the channel depth. We also observe that, the drain current levels decrease as the implant damage traps depth increases due to increasing channel resistance brought about by increased implant damage traps. At any depth beyond the implant damage traps depth of  $3.0\ \mu\text{m}$ , the hysteresis and drain current levels virtually stay the same as can be seen from Figure B.19. This is due to the spatial distribution of the drain current as shown in current contour figures above. It appears that the appropriate combination of implant damage traps depth and lateral straggle width give rise to the hysteresis in the drain I-V curves.

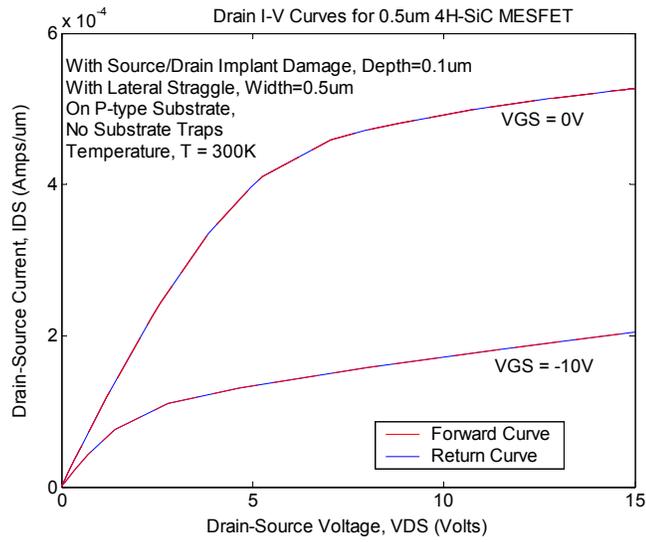
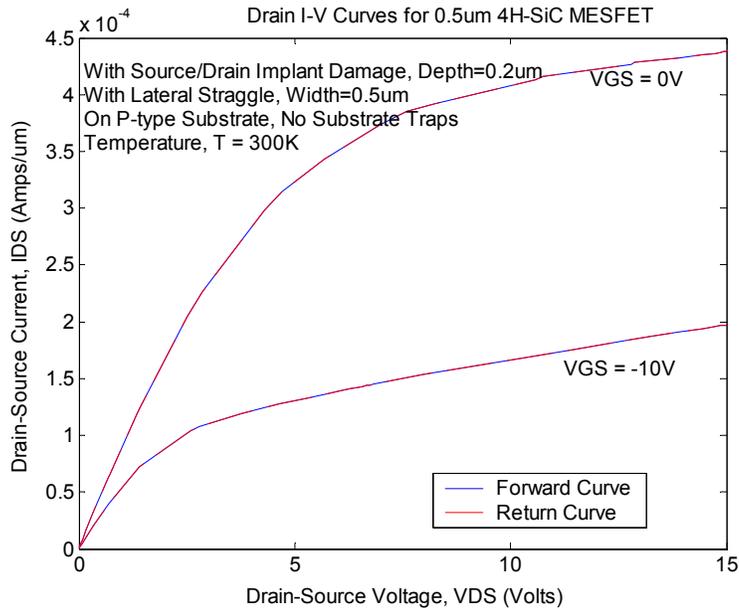
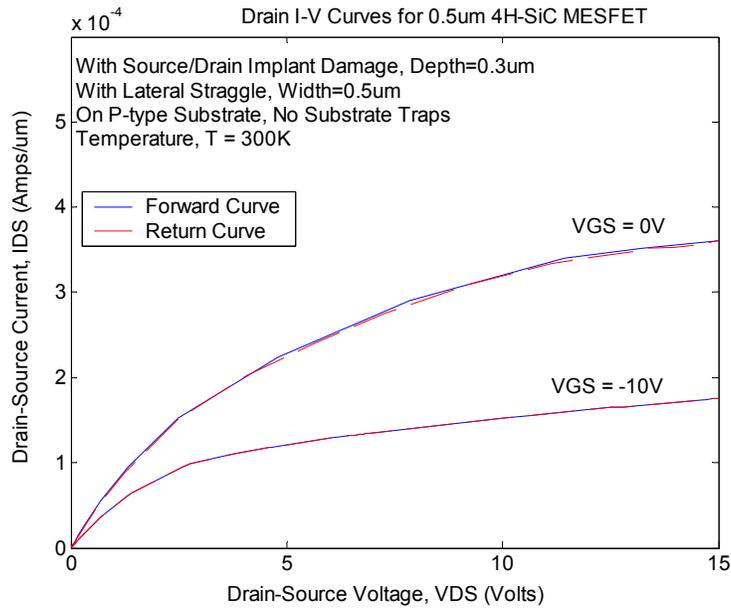


Figure B.17: Drain I-V curves for simulation MESFET with source/drain implant damage traps depth = 0.1  $\mu\text{m}$ .

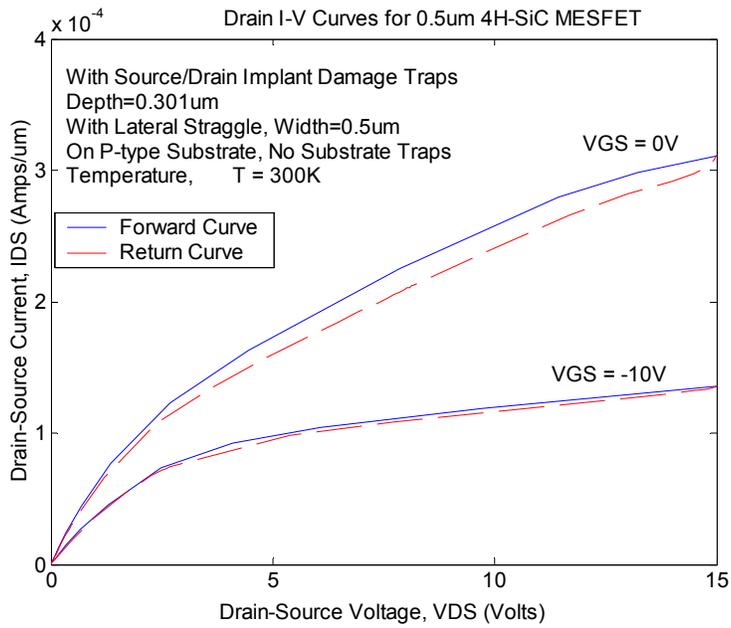


(a)

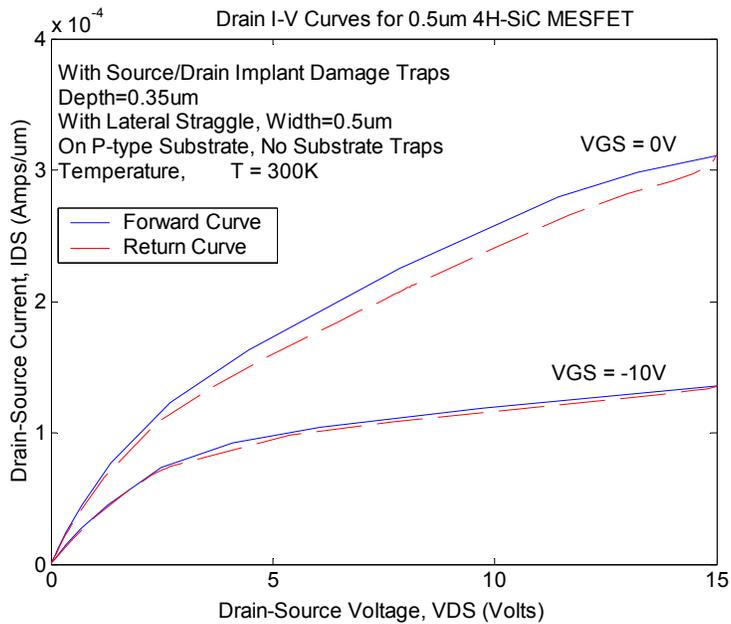


(b)

Figure B.18: Drain I-V curves for simulation MESFET with (a) source/drain implant damage traps depth = 0.2  $\mu\text{m}$  (b) source/drain implant damage traps depth=0.3  $\mu\text{m}$ .



(a)



(b)

Figure B.19: Drain I-V curves for simulation MESFET with (a) source/drain implant damage traps depth = 0.301  $\mu\text{m}$  (b) source/drain implant damage traps depth = 0.35  $\mu\text{m}$

## B.5 Effects of Source/Drain Implant Damage Trap Distribution on I-V Curves

This section investigates the effect of source/drain implant damage traps on drain I-V curves when the implant damage is just restricted to the lateral straggle region in the channel and when the implant damage covers the entire source and drain regions with their attendant lateral straggle. Figures B.20 (a) and (b) show the situation when the implant damage traps are restricted to the lateral straggle areas at the source and drain respectively, and Figures B.21 (a) and (b) show the corresponding drain I-V characteristics. In both situations, the implant damage width and depth used in the simulation were  $0.5\ \mu\text{m}$  and  $0.4\ \mu\text{m}$  respectively.

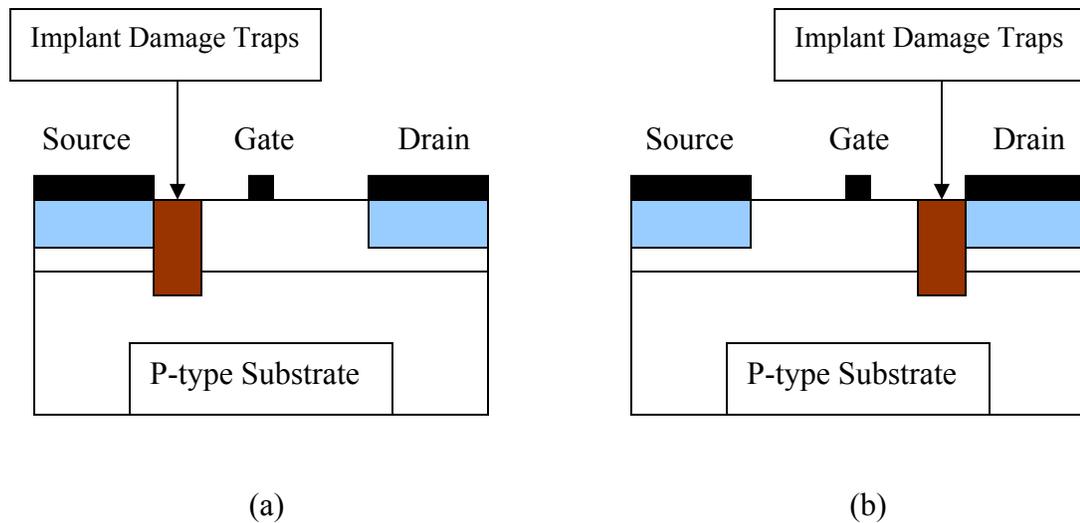
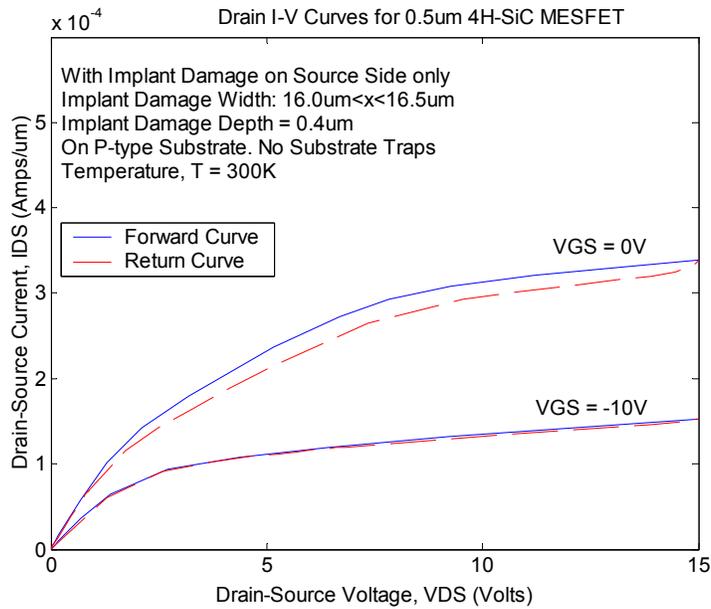
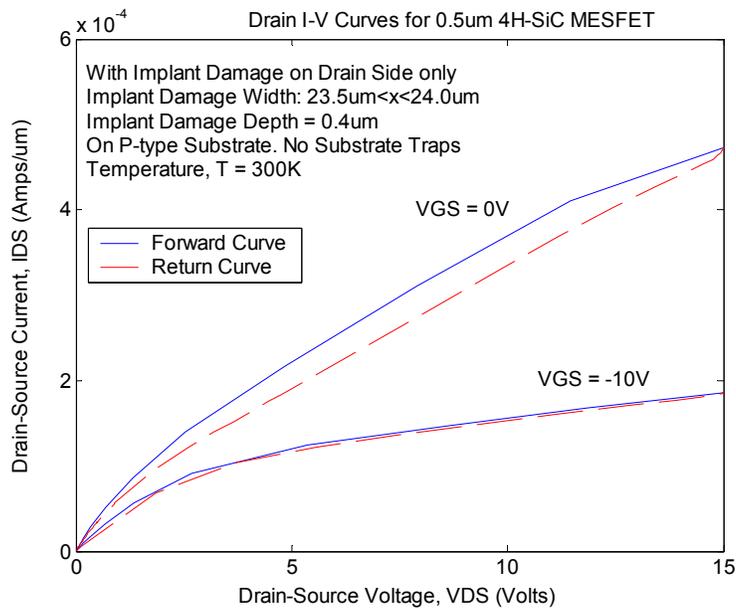


Figure B.20: MESFET with implant damage restricted to (a) the source only and (b) the drain only.



(a)



(b)

Figure B.21: Simulated drain I-V curves for a MESFET with implant damage traps restricted to (a) the source side only and (b) the drain side only.

From Figure B.21 we see that when the implant damage is restricted to the source side only, the degree of hysteresis and current levels are lower than when the implant damage is only restricted to the drain side. Since implant damage introduces resistance into the channel, this shows that source resistance has more deleterious effect on the drain I-V characteristics than the drain resistance. In particular, we observe from Figure B.21 that the implant damage on the source side drastically reduces the drain current, which has the effect of reducing the transistor output power. The above scenario explains why in MESFET design the gate is shifted towards the source to reduce source resistance. This has the added effect of increasing the drain breakdown voltage since the distance between the gate and the drain is increased. Figure B.22 (a) and (b) show the case where the implant damage covers the entire source and drain regions respectively with lateral straggle included indicated by the dotted lines, and Figures B.23 (a) and (b) show the corresponding drain I-V characteristics.

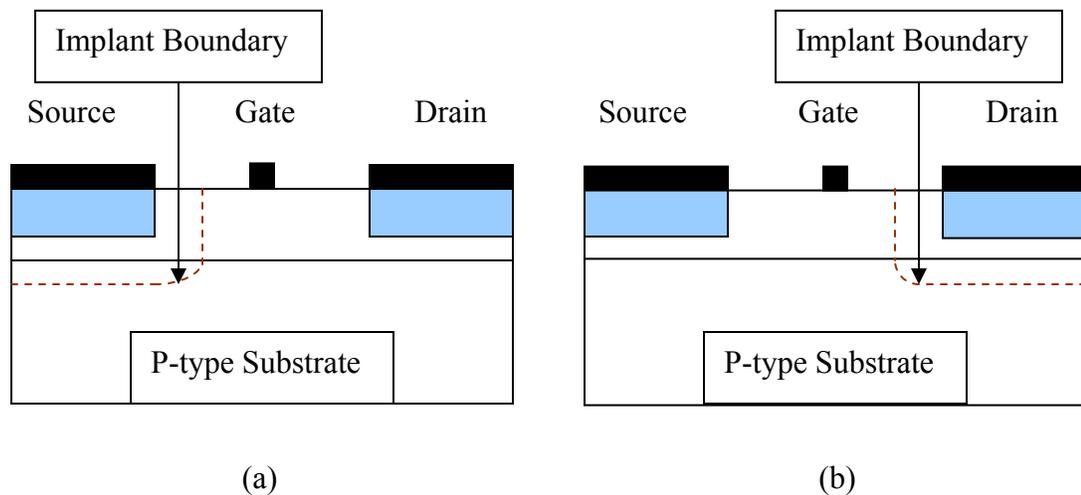
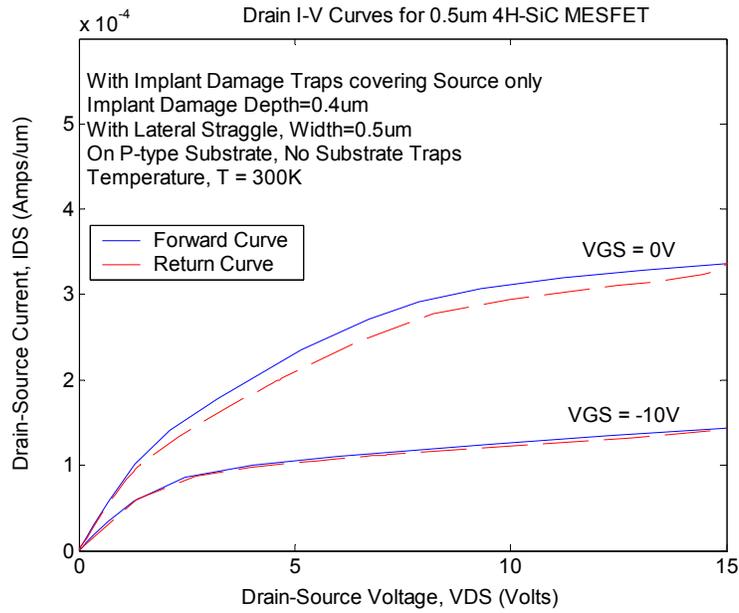
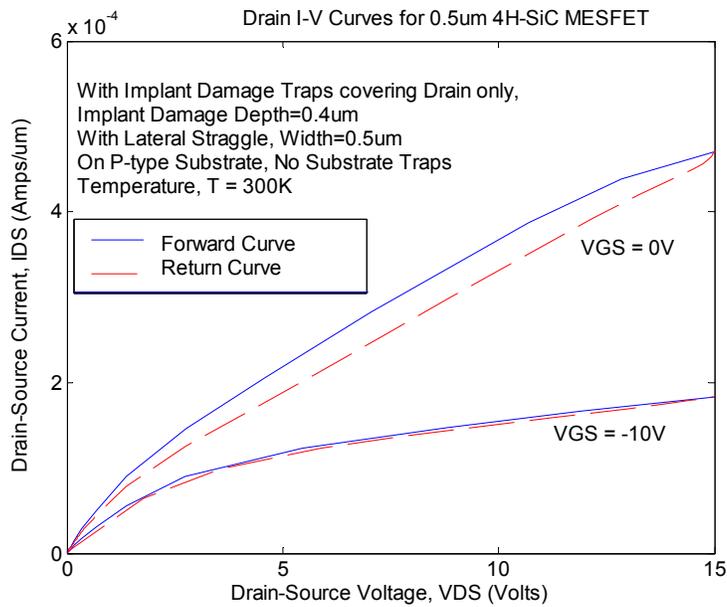


Figure B.22: MESFET with implant damage covering (a) the source only and (b) the drain only.



(a)



(b)

Figure B.23: Simulated drain I-V curves for MESFET with implant damage traps covering (a) only the source and (b) only the drain.

Comparing Figures B.21a and B.23a we observe that the degree of hysteresis and current levels are the same. When we also compare Figure B.21b to Figure B.23b, we observe again that the degree of hysteresis and current levels are the same. These observations further reinforce our earlier observation that it is the traps due to the lateral straggle of implanted species that control the hysteresis in the drain I-V characteristics and drain current levels. No hysteresis appears in the drain I-V curves when width of the lateral straggle is reduced to zero. Figures B.24 (a) and (b) show the case where the implant damage is restricted to the lateral straggle area in the channel on both the source and drain sides, and where the implant damage covers both the source and drain regions with a lateral straggle of  $0.5 \mu\text{m}$ , respectively. Figures B.25 (a) and (b) show the simulated drain I-V curves for the two situations respectively.

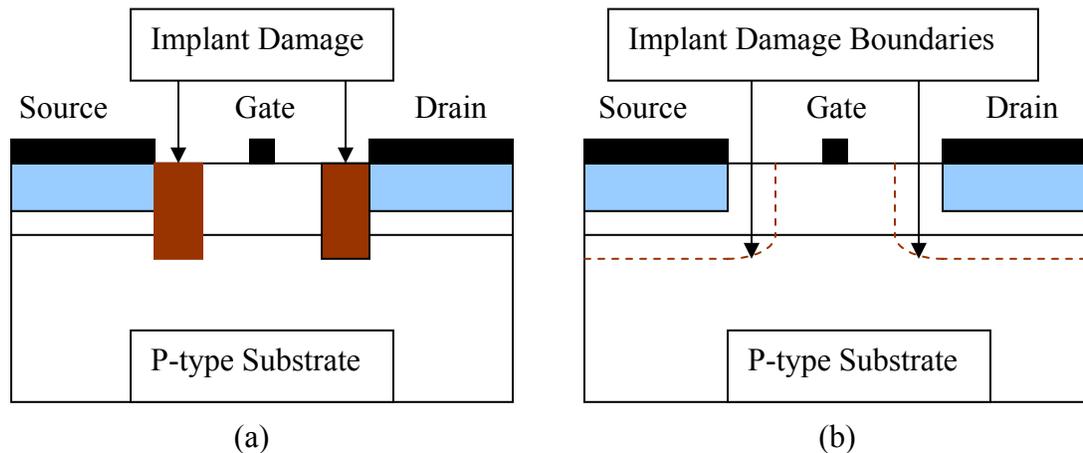


Figure 2.24: MESFET with (a) implant damage restricted to the lateral straggle area in the channel on both source and drain sides (b) implant damage covering both the source and drain. In both cases the depth of implant damage is  $0.4 \mu\text{m}$  and lateral straggle width =  $0.5 \mu\text{m}$ .

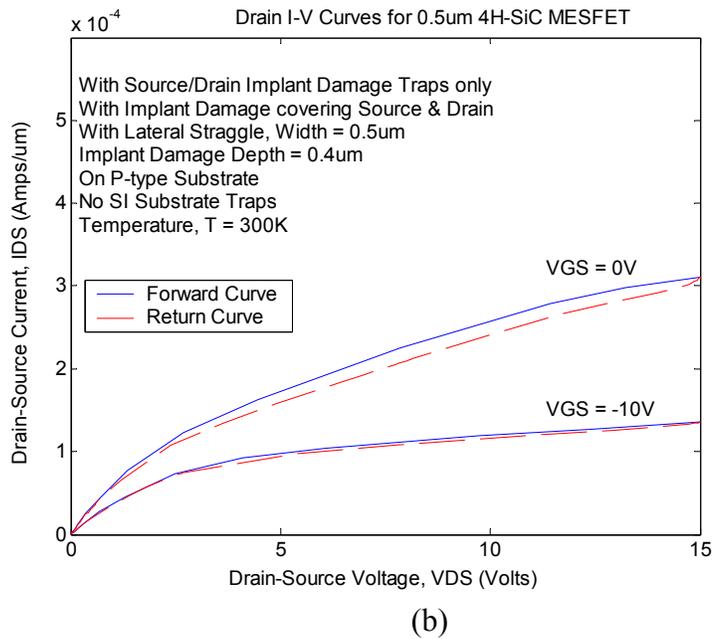
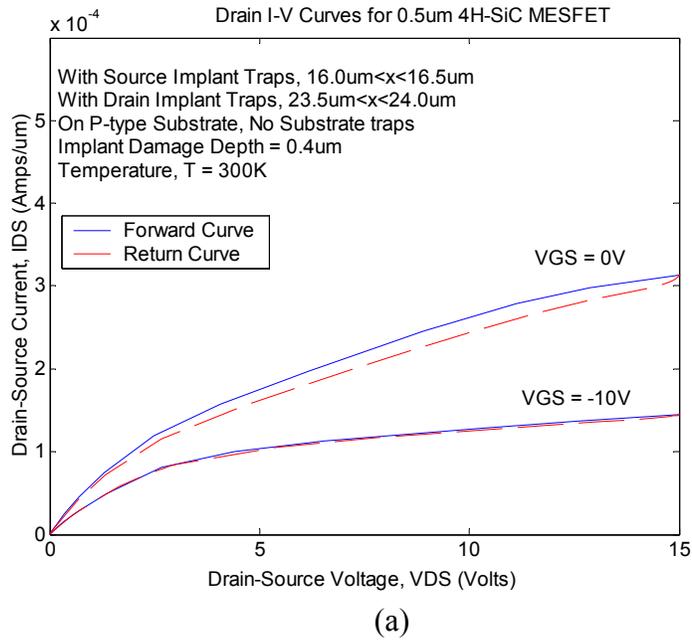


Figure B.25: Simulated drain I-V curves for MESFET (a) with implant damage traps restricted to the lateral straggle area in the channel on both the source and drain sides and (b) with implant damage traps covering both the source and drain. In both cases the implant damage depth is 0.4  $\mu$ m and lateral straggle width = 0.5  $\mu$ m.

From Figures B.25 (a) and (b) we see that the degree of hysteresis and drain current levels are the same for the case where the implant damage is restricted to the lateral straggle areas at source and drain sides and for the case where the implant damage covers both the source and drain regions entirely. In both cases the depth of the implant damage is  $0.4\ \mu\text{m}$  and the lateral straggle width is  $0.5\ \mu\text{m}$ . This further supports the observation that, the hysteresis in the drain I-V curves of MESFET with source/drain residual implant damage traps is due mainly to the traps due to the lateral straggle since without the lateral straggle traps no hysteresis appears in the I-V characteristics as shown in Figure B.8. In addition as observed in section B.1.3, for lateral straggle width less than  $0.2\ \mu\text{m}$  no hysteresis appears in the drain I-V curves while hysteresis appears in the I-V curves when the lateral straggle width is greater than  $0.2\ \mu\text{m}$ .

### **B.6 Effect of Displacement from the Device Surface of Implant Damage Traps on Drain I-V Curves**

In this section we investigate the effect the displacement from the device surface of the implant damage traps has on the drain I-V characteristics. Figure B.26 shows the case where the implant damage traps is restricted to the lateral straggle region at the source and drain areas with a width of  $0.5\ \mu\text{m}$  and a depth of  $0.4\ \mu\text{m}$  as the damaged area is displaced from the device surface. The I-V curves for the case where the implant damage areas are displaced a distance of  $0.02\ \mu\text{m}$  and  $0.0499\ \mu\text{m}$  from the device surface are shown in Figures B.27 and B.28 respectively. We see that the degree of hysteresis, and current levels are the same as the case, where the distribution of implant damage starts from the surface as shown in Figure B.24a and Figure B.25a.

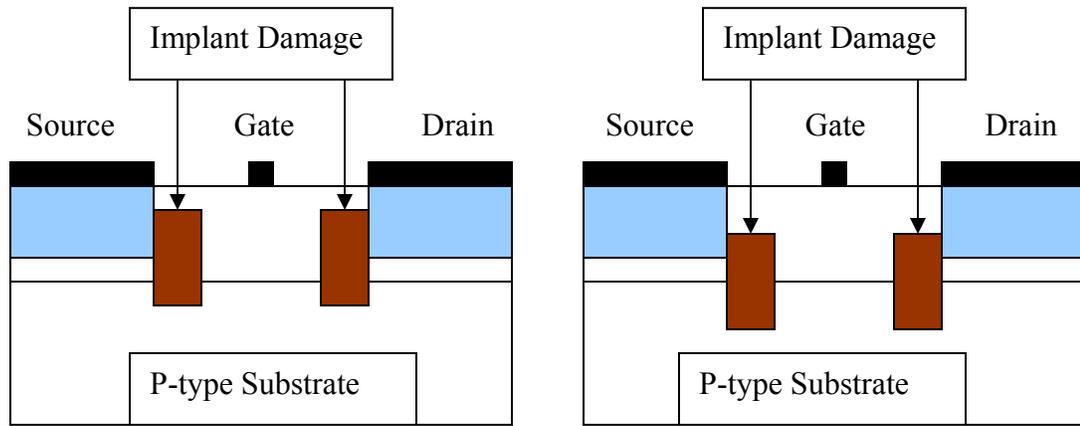


Figure B.26: Structure of simulation MESFET with implant damage areas displaced from the device surface.

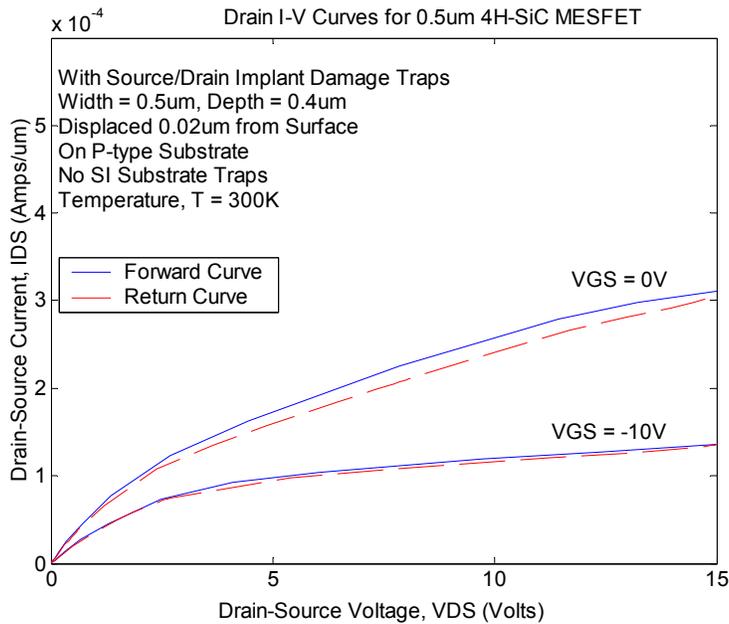


Figure B.27: Simulated drain I-V curves for MESFET with implant damage traps displaced 0.02  $\mu\text{m}$  from the device surface.

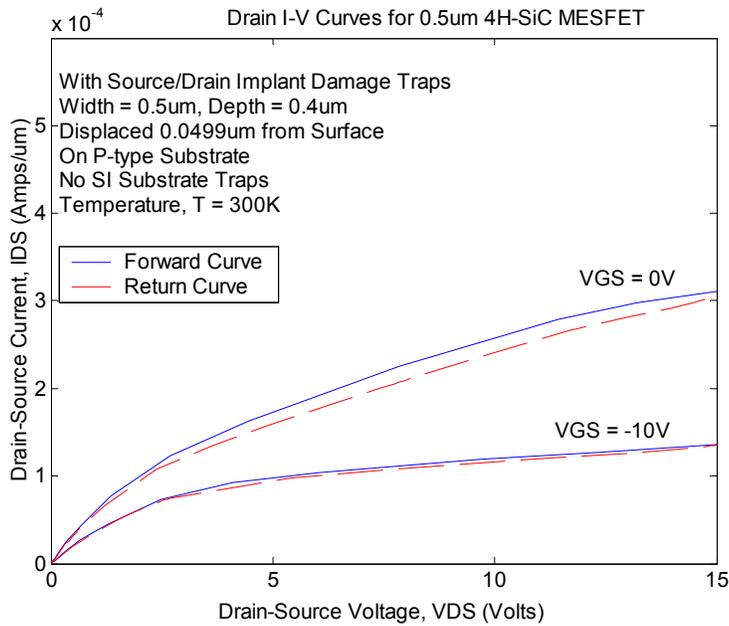
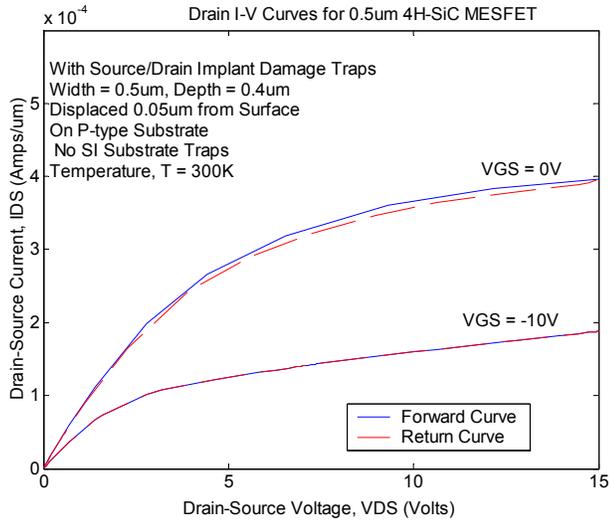


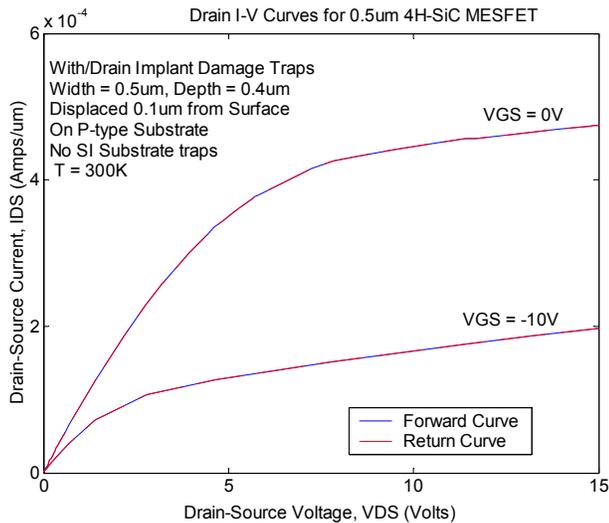
Figure B.28: Simulated drain I-V curves for MESFET with implant damage traps displaced 0.0499  $\mu\text{m}$  from the device surface.

Figures B.29 (a) and (b) show the case where the implant damage traps are displaced a distance of 0.05  $\mu\text{m}$  and 0.1  $\mu\text{m}$  from the surface respectively. As the displacement of implant damage traps increases from the device surface to about 0.0499  $\mu\text{m}$  from the surface, the degree of hysteresis and current levels remain the same. Somewhere between 0.0499  $\mu\text{m}$  and 0.05  $\mu\text{m}$  the hysteresis begin to decrease and the current levels increase and finally the hysteresis disappear completely from the drain I-V curves. This is because as the implant damage traps distribution is pushed away from the surface, it is removed further away from the current flow regions in the channel. As a result, fewer electrons flow through the implant damage areas and therefore electron

trapping and emission are reduced. Hence, hysteresis decrease and current levels increase since channel resistance decrease as the implant damage areas are pushed away from the channel area.



(a)



(b)

Figure B.29: Simulated drain I-V curves for MESFET with implant damage traps displaced (a) 0.05 µm and (b) 0.1 µm from the device surface.

Figure B.30 shows the situation in which the implant damage covers the source and drain regions with a lateral straggle of  $0.5 \mu\text{m}$  and depth of  $0.4 \mu\text{m}$  and displaced at some distance from the device surface. Figures B.31 (a), (b), Figures B.32 (a), and (b) show the drain I-V characteristics for cases in which the source/drain implant damage is displaced  $0.02 \mu\text{m}$ ,  $0.0499 \mu\text{m}$ ,  $0.05 \mu\text{m}$ , and  $0.1 \mu\text{m}$  from the device surface respectively. Comparing Figure B.31 to Figures B.28 and B.29, we see that it does not matter whether the implant damage covers the entire source and drain regions or the damage is restricted to the channel in the lateral straggle area as shown in Figure B.26 and already observed above. In both situations the current levels and degree of hysteresis are the same. This is again due to the fact that the current flows between the inside edges of the source and drain as shown in Figure B.33. Figure B.33b shows that much of the drain current is restricted to the channel area although the 2-D current contours in Figure B.33a shows substantial substrate current.

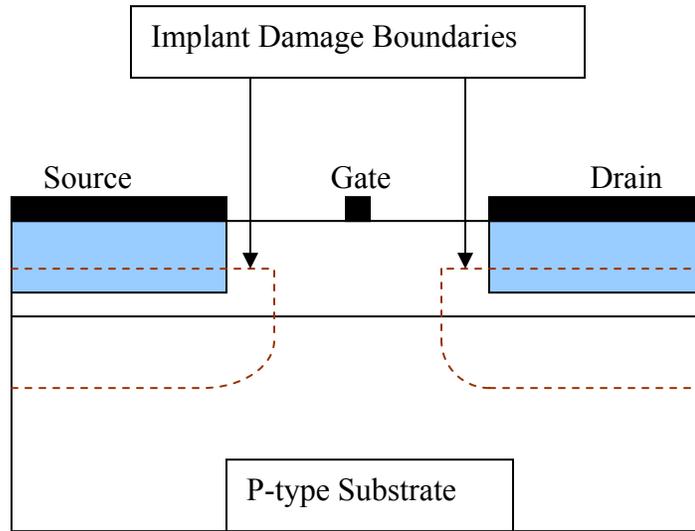
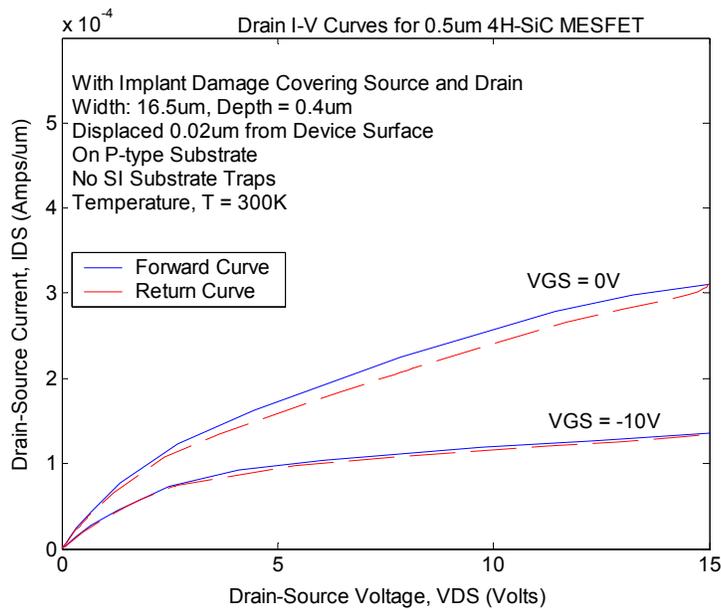
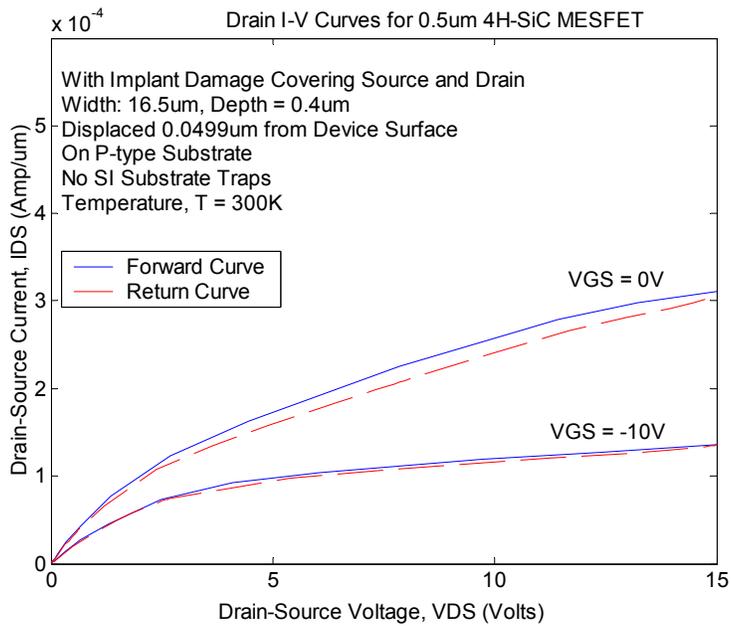


Figure B.30: Structure of MESFET with source/drain implant damage displaced a given distance from the device surface.

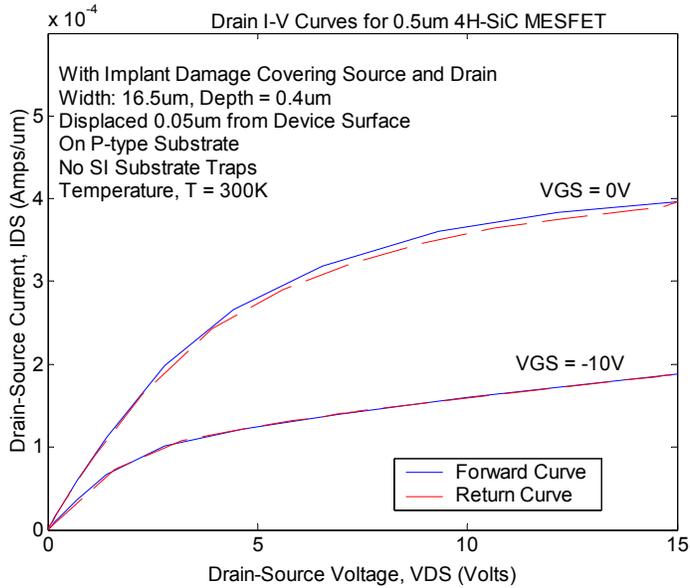


(a)

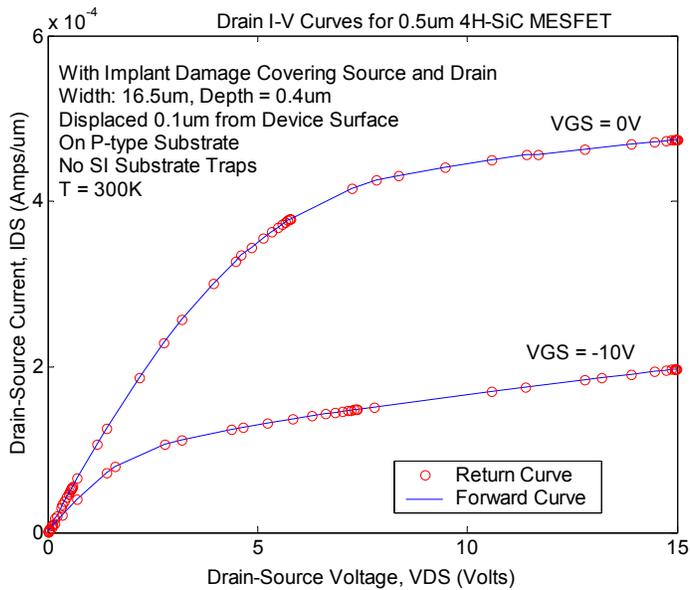


(b)

Figure B.31: Simulated drain I-V curves for MESFET with implant damage covering source and drain regions and displaced (a) 0.02  $\mu\text{m}$  and (b) 0.0499  $\mu\text{m}$  from the device surface.

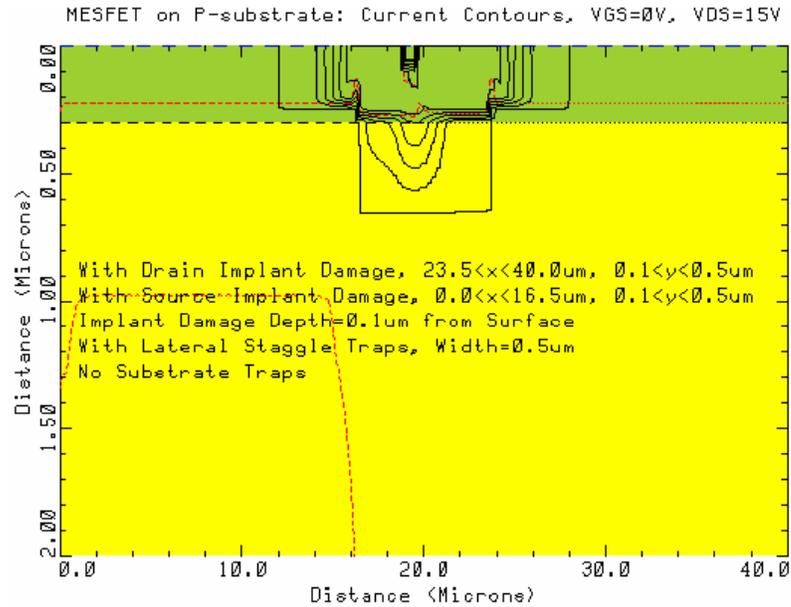


(a)



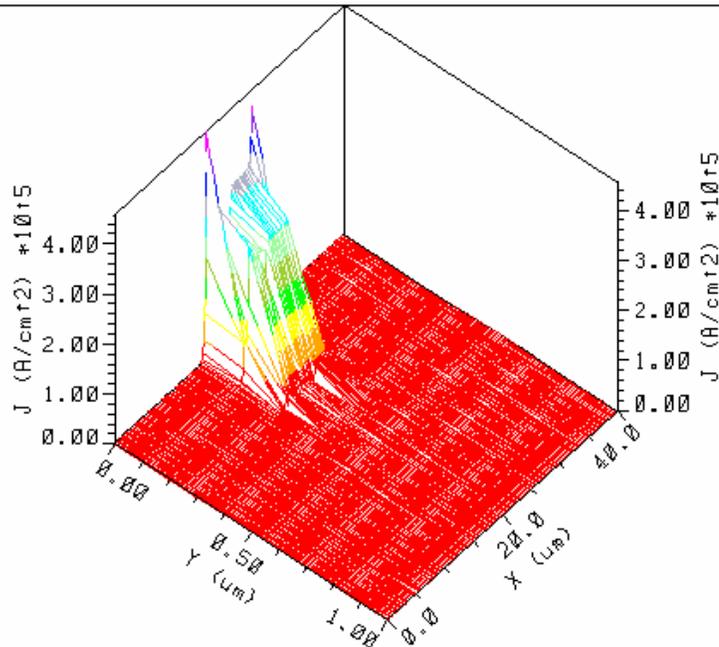
(b)

Figure B.32: Simulated drain I-V curves for MESFET with implant damage covering source and drain regions and displaced (a) 0.05  $\mu\text{m}$  and (b) 0.1  $\mu\text{m}$  from the device surface.



(a)

3-D Current Plot for  $0.5 \mu m$  4H-SiC MESFET,  $V_{GS}=0V$ ,  $V_{DS}=15V$



(b)

Figure B.33: (a) 2-D current contours for MESFET with  $V_{GS} = 0 V$ ,  $V_{DS} = 15 V$   
 (b) 3-D current plot for MESFET with  $V_{GS} = 0 V$ ,  $V_{DS} = 15 V$ . Note that the 3-D plot shows that much of the current is restricted to the channel.

Figure B.34 below shows the trap occupation for the case where the traps cover the source and drain regions with a depth of  $0.4 \mu\text{m}$ , a lateral straggle of  $0.5 \mu\text{m}$  and displaced a distance of  $0.1 \mu\text{m}$  from the device surface. If we compare Figure B.33b to Figure B.34, we see that much of the current flows close to the device surface and that as the trap distribution is displaced from the device surface the traps are removed from the current flow volume. Thus less current flows through the implant damage trap distribution and hence the resistance presented by the traps. There is reduced interaction between the current and trap distributions. This causes increased current flow and reduced current hysteresis as the implant damage trap distribution is further displaced from the device surface as shown in Figures B.31 and B.32 above.

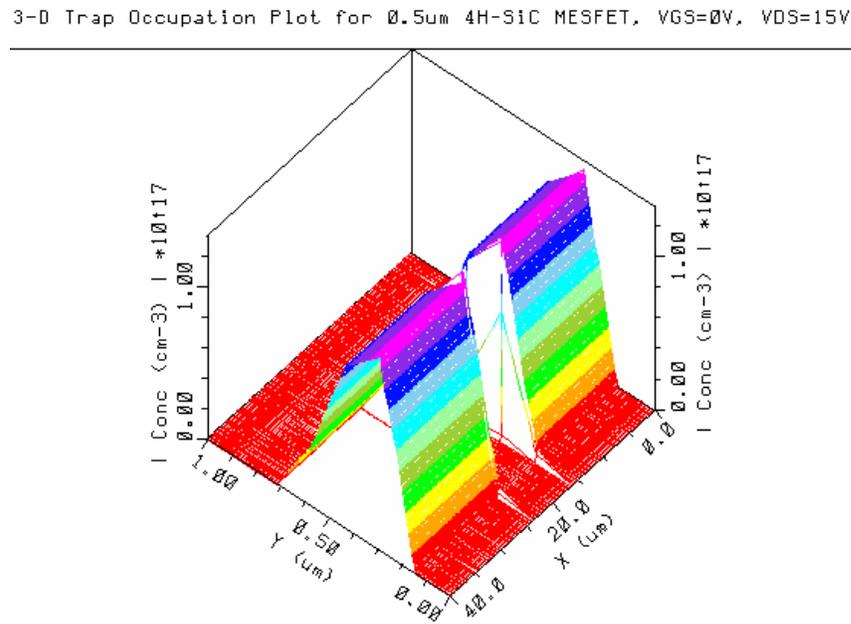


Figure B.34: 3-D trap occupation plot for the case where the implant damage traps cover the source and drain and displaced  $0.1 \mu\text{m}$  from the device surface. Note that there is virtually no interaction between the current and trap distributions, leading to the absence of hysteresis in the drain I-V curves.

Figure B.35 (a) and (b) below depicts the cases where the implant damage traps are displaced  $0.02 \mu\text{m}$  from the surface and restricted to the source side and drain side respectively, with a lateral straggle of  $0.5 \mu\text{m}$ . Figures B.36 (a) and (b) show the corresponding drain I-V curves. The displacement distance of  $0.02 \mu\text{m}$  from the device surface is selected because the same current level and degree of hysteresis in the drain current are obtained for displacement of  $0.0 \mu\text{m}$  to  $0.0499 \mu\text{m}$  from the device surface. The degree of hysteresis begin to decrease (and eventually vanishes) and drain current levels begin to increase only when the displacement of the trap distribution from the device surface is  $0.05 \mu\text{m}$  and greater. Figure B.36a shows that, relative to Figure B.27 in which the channel implant damage is at both the source and drain, when the implant damage is only at the source the current levels and the degree of hysteresis, particularly at  $V_{GS} = 0 \text{ V}$ , are slightly increased. On the other hand as shown in Figure B.36b, when the channel implant damage is only at the drain side the drain current levels and the degree of hysteresis are greatly enhanced. These observations further give evidence to the fact that it is the source resistance due to the source implant damage that controls the current levels and degree of hysteresis. When the implant damage is only at the source side, less current flows due to higher channel resistance brought about by the relatively high source resistance, leading to relatively smaller drain current hysteresis. When the implant damage is only at the drain side, more current flows due to decreased channel resistance. Increased current levels imply more free electrons to be trapped by implant damage traps, and hence higher degree of drain current hysteresis, as can be seen in Figure B.36b.

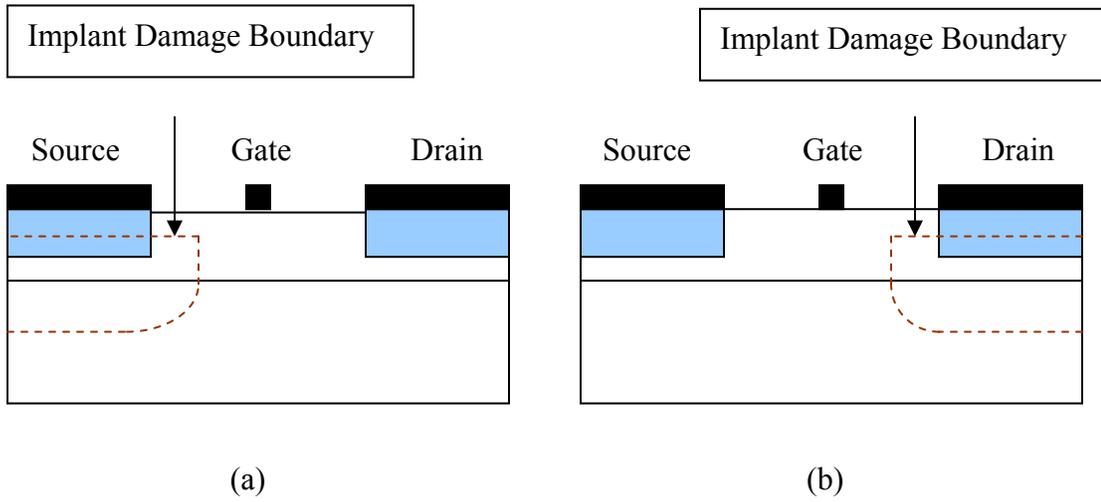
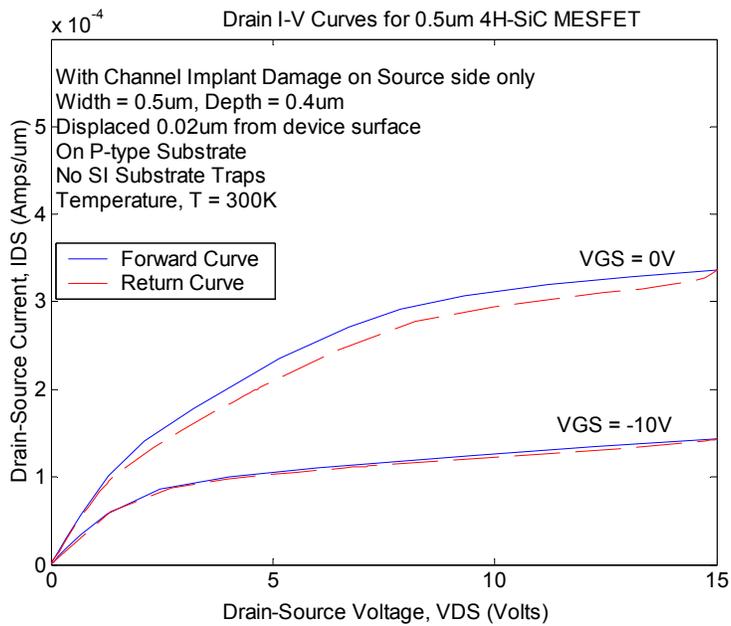
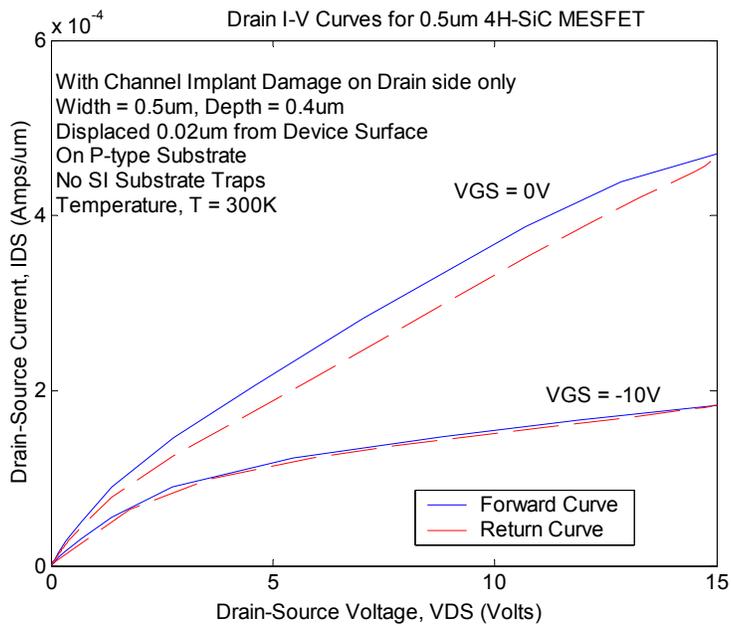


Figure B.35: Structure of MESFET with (channel) implant damage traps displaced  $0.02 \mu\text{m}$  below the device surface (a) on source side only and (b) on drain side only.



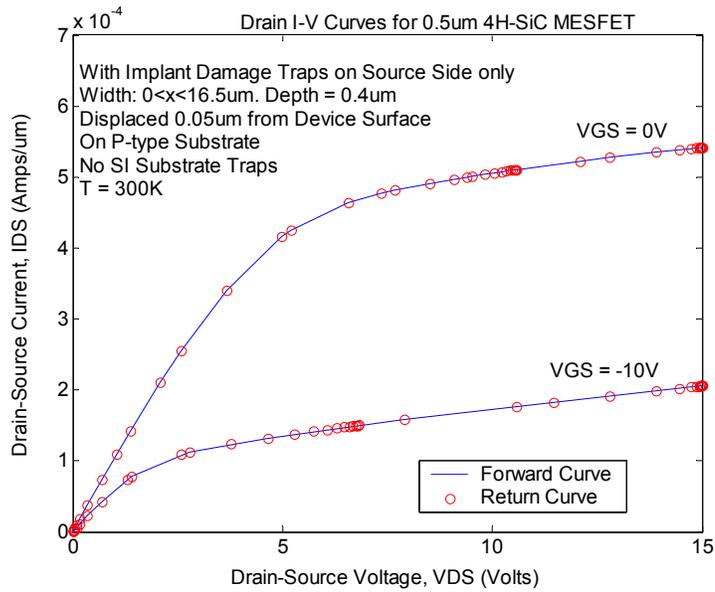
(a)



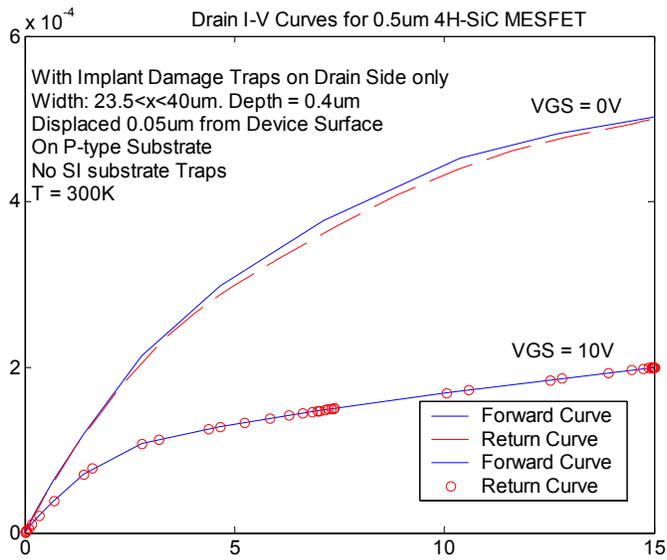
(b)

Figure B.36: Simulated drain I-V curves for MESFET with channel implant damage traps displaced  $0.02 \mu\text{m}$  from the device surface (a) on source side only and (b) on drain side only.

As already established above, it does not really matter whether the implant damage covers the entire source and drain regions with their attendant lateral straggle or the damage is restricted to the lateral straggle, the I-V characteristics are similar. Therefore by extension, the I-V curves in Figure B.36, also applies to the case where the implant damage traps are restricted to the lateral straggle (width = 0.5  $\mu\text{m}$ , depth = 0.4  $\mu\text{m}$ ). Figure B.37 below shows the I-V characteristics for the scenario in Figure B.35 where the implant damage is displaced 0.05  $\mu\text{m}$  from the device surface. If we compare the I-V curves in Figure B.37 to those in Figure B.32a for the case where the implant damage traps cover both the source and drain regions, we observe that all the hysteresis in Figure B.32a for  $V_{GS} = 0 \text{ V}$  is due to the drain side implant damage traps. The source side implant damage traps do not contribute any hysteresis as seen from Figure B.37a. It can also be seen that the degree of hysteresis in Figure B.37b is about the same as that in Figure B.32a although the current levels in Figure B.37b are higher due to the reduced channel resistance presented by the implant damage traps. The absence of hysteresis in Figure B.37a is due to the fact that there is little or no interaction between the trap and current distributions as seen from the careful study of Figure B.38. In order for hysteresis to occur, the current and trap distributions should overlap. In addition the current levels should be such that there are enough free electrons to be trapped.



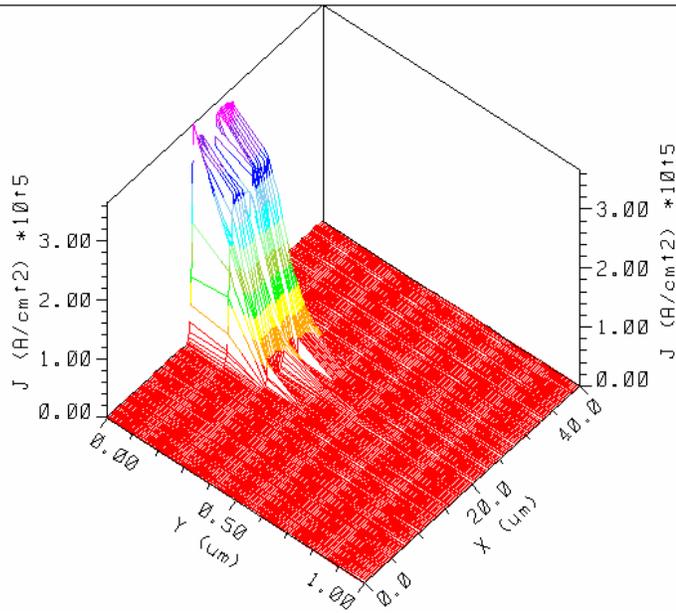
(a)



(b)

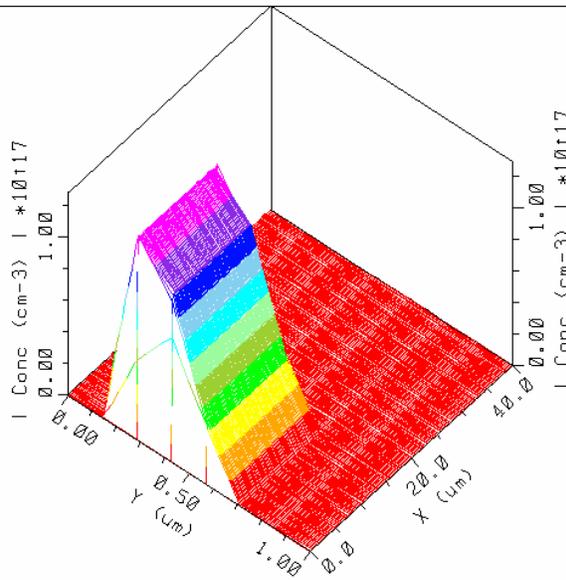
Figure B.37: Simulated drain I-V curves for MESFET with (a) implant damage traps covering the source only with  $0.5\mu\text{m}$  lateral straggle (b) covering the drain only with  $0.5\mu\text{m}$  lateral straggle. All implants are displaced  $0.05\mu\text{m}$  from the device surface.

3-D Current Plot for 0.5um 4H-SiC MESFET, VGS=0V, VDS=15V



(a)

3-D Trap Occupation Plot for 0.5um 4H-SiC MESFET, VGS=0V, VDS=15V



(b)

Figure B.38: (a) 3-dimensional current plot for MESFET with implant damage traps on the source side with 0.5  $\mu\text{m}$  lateral straggle and displaced 0.05  $\mu\text{m}$  from device surface (b) the corresponding trap occupation.